Project assignment #2 assigned 2/28/01 due 3/7/01

a) Simulate your circuit using SPICE. Use the p-MOS device parameters provided below.

b) Simulate a DC test of your circuit using the HP4145 parameter analyzer. Apply a variable VAR1 and VAR2 using the following analysis statement.

```
.DC VAR1 0 -15 -0.5 VAR2 0 -15 -5
```

c) Check the operation of the circuit by applying a series of input signals versus time. Perform a transient analysis and plot the input signals as well as the corresponding output signals.

d) Repeat your simulations with a p-MOS threshold voltage of -5 Volt for \( V_{SB} = 0 \) V. Find the minimum power supply voltage needed to make the circuit function.

NOTE: Use the following PSPICE model for the pMOSFETs:

```
.MODEL PFET PMOS (LEVEL=2 L=20u W=20u VTO=-1.44 KP=8.64E-6 + NSUB=2E15 TOX=80n)
```
Common problems when simulating circuits using PSPICE

General problems

PSPICE can not handle floating nodes (i.e. not connected nodes)
While PSPICE provides an error message for errors in node lists and refuses to continue the simulation, it does not catch floating nodes which occur when a node is shared by transistors only and all transistors to that node are turned off. You will get a cryptic message instead. This problem can be resolved by adding a high impedance (for instance a 100 MΩ resistor) between that node and ground.

PSPICE can pose problems when applying a current source to the drain/collector of the transistor.
Since the transistor is modeled as a voltage controlled current source one would effectively have two current sources in series with each other. This can cause numeric instabilities. The problem can be avoided by using a large voltage source in series with a large resistor instead of a current source or by adding a resistor from the node connecting the current source to ground.

Specific problems when simulating flip-flops and ringoscillators

Flip-flops and ringoscillators made of identical invertors pose problems since PSPICE comes up with the unstable DC bias conditions for the flip-flop (with both outputs at the same voltage) or a non-oscillating solution for the ringoscillator. This can be fixed by providing an asymmetry in the circuit making one transistor larger than the others with the same nominal value or by adding asymmetric loading.
MOSFET syntax

\[ M\text{<name>} \ <\text{drain node}> \ <\text{gate node}> \ <\text{source node}> \ <\text{bulk/substrate node}> \]
+ \ <\text{model name}> \ [L=<value>]\[W=<value>]\[AD=<value>]\[AS=<value>] \]
+ \ [PD=<value>]\[PS=<value>]\[NRD=<value>]\[NRS=<value>] \]
+ \ [NRG=<value>]\[NRB=<value>] \]

where L is the gate length, W the gate width, AD the drain area, AS the source area
PD is the drain perimeter, PS is the source perimeter

d example:

M1 3 2 1 0 PFET L=20u W=120u
.MODEL PFET PMOS (LEVEL=2 L=20u W=20u VTO=-1.44 KP=8.64E-6
+ NSUB=2E15 TOX=80n)

Model parameter list

LEVEL=2 ; model type
L=20u ; channel length
W=20u ; channel width
LD= ; lateral diffusion (length)
WD= ; lateral diffusion (width)
VTO=-1.44 ; zero-bias threshold
KP=8.64E-6 ; transconductance
GAMMA= ; bulk threshold parameter
PHI= ; surface potential
LAMBDA= ; channel length modulation (LEVEL = 1 or 2)
RD= ; drain ohmic resistance
RS= ; source ohmic resistance
RG= ; gate ohmic resistance
RB= ; bulk ohmic resistance
RDS= ; drain-source shunt resistance
RSH= ; drain source diffusion sheet resistance
IS= ; bulk p-n saturation current
JS= ; bulk p-n saturation current/area
PB= ; bulk p-n potential
CBD= ; bulk-drain zero-bias p-n capacitance
CBS= ; bulk source zero-bias p-n capacitance
CJ= ; bulk p-n zero-bias bottom capacitance
CJSW= ; bulk p-n zero-bias perimeter capacitance
MJ= ; bulk p-n bottom grading coefficient
MJSW= ; bulk p-n sidewall grading coefficient
FC= ; bulk p-n forward-bias capacitance coefficient
CGSO= ; gate-source overlap capacitance/channel width
CGDO= ; gate-drain overlap capacitance/channel width
CGBO= ; gate-bulk overlap capacitance/channel width
NSUB=2E15 ; substrate doping density
NSS= ; surface state density
NFS= ; fast surface state density
TOX=80n ; oxide thickness
TPG= ; gate material type (0=aluminum)
XJ= ; metallurgical junction depth
UO= ; surface mobility
UCRIT= ; mobility degradation critical field (LEVEL=2)
UEXP= ; mobility degradation exponent (LEVEL=2)
UTRA= ; not used
VMAX= ; maximum drift velocity
NEFF= ; channel charge coefficient
XQC= ; fraction of channel charge attributed to the drain
DELTA= ; width effect on threshold
THETA= ; mobility modulation (LEVEL=3)
ETA= ; static feedback (LEVEL=3)
KAPPA= ; saturation field feedback (LEVEL=3)
KF= ; flicker noise coefficient
AF= ; flicker noise exponent