Complete the top portion of the bubble sheet with your student ID number and your name. Sign your name in the blank space at the bottom of the sheet. In the "1 2 3 4" columns, put a "0" in column 1 and your lab section number in columns 2, 3 and 4.

Use a number 2 pencil to clearly select your answer. If you need more space to work a problem, use the back of an exam page. You have 50 minutes.

**Good Luck!**

**Question 1.** (3 points) When using the UART, which of the following would be considered a control register:
(a) IIR  (b) MSR  (c) LCR  (d) THR  (e) None of these.

**Question 2.** (3 points) When using the UART, which of the following would be considered a status register:
(a) IIR  (b) MCR  (c) LCR  (d) RBR  (e) None of these.

**Question 3.** (5 points) When discussing the RS 232 standard, it was pointed-out that only three signal lines are needed to make a connection between a computer and a terminal. Which of the following would be used?
(a) RD  (b) CTS  (c) RTS  (d) DTR  (e) a and d.

**Question 4.** (5 points) A sequence of code that requires 38 machine cycles to execute is run on a 25MHz processor. How many seconds does it take to execute the code sequence?
(a) 950 sec.  (b) 1.52 msec.  (c) 950 μsec.  (d) 1.52 μsec.  (e) 152 nsec.

**Question 5.** (5 points) The value of MBIT is a mask that is set with an EQU. Which of the following lines of code would set bits in D0 according to the position of 1’s in MBIT, without modifying the rest of the bits in D0.
(a) AND #MBIT,D0  (d) OR #MBIT,D0
(b) AND MBIT,D0  (e) None of these.
(c) BSET #MBIT,D0

**Question 6.** (5 points) When handling a small number of I/O devices in a system (less than 5) the effect of using a daisy chain can be achieved by using:
(a) Priority Polling  (d) a or b.
(b) A priority interrupt controller  (e) b or c.
(c) Round-robin polling
Questions 7-10. Consider an asynchronous serial communications system running at 2400 baud. This system is set-up to use 1 stop bit, 8 data bits and even parity. The line is normally held at a logical "1". Assume that the character "C" (43H) is to be transmitted on the line.

Question 7. (3 points) What is the value of the parity bit?
(a) 0 (b) 1 (c) Not enough information.

Question 8. (5 points) What is the "bit period" for this communications set-up? (That is, how long does it take to transmit one bit?)
(a) 104.17 μsec. (b) 104.17 msec. (c) 416.67 μsec. (d) 4.167 msec. (e) None of these.

Question 9. (5 points) At most, how many characters can be transmitted per second?
(a) 218 (b) 240 (c) 300 (d) 342 (e) 2400

Question 10. (5 points) The frame that represents the transmission of the "C" is (from first bit sent on the left to last bit sent on the right, where the "P" represents the value of the parity bit):
(a) 01000011P1 (c) 001000011P1 (e) 01000011P
(b) 11000010P1 (d) 011000010P1

Question 11. (5 points) Which of the following statements about interrupt handlers is true?
(a) The interrupt handler can be invoked by hardware or software.
(b) The interrupt handler is a procedure call.
(c) Interrupt handlers must disable interrupts.
(d) The interrupt handler needs to save and restore any registers it uses.
(e) b and d are true.

Questions 12-13. For the MB5 68000 system that you have been using, a new interrupt handler is written to replace the interrupt handler associated with the level 4 interrupt auto-vector. The name of this new interrupt handler is NewHandler and the linker has assigned it to be at location $105B0A.

Question 12. (5 points) To get the processor to execute the handler, the value $105B0A must be written to a location in memory. In which range of addresses below would you expect to write this value?
(a) $0-$3FF (c) $105000-$106000 (e) None of these.
(b) $100000-$100200 (d) $1FF000-$1FFFFF

Question 13. (5 points) If NewHandler is the interrupt service routine for a UART, which of the following registers would you expect to write before NewHandler could be invoked?
(a) LCR (b) SR (c) IER (d) a and b. (e) b and c.
Question 14. (5 points) The fact that the DMA controller is capable of becoming a bus master makes which of the following possible?
(a) Block data transfers that do not require the CPU to load a Program Counter value for each byte or word of data that is transferred.
(b) A data transfer between memory and a device data register bypasses the CPU.
(c) The DMA controller could steal bus cycles with little impact on the CPU’s performance.
(d) It takes fewer bus cycles to get a byte of data from a device interface to memory.
(e) All of the above.

Question 15. (5 points) In the 68000, to provide mutual exclusion when a program wants to enter a critical section, which of the following statements is true?
(a) A CMPI.B instruction would be executed.
(b) A TAS instruction would be executed.
(c) A V operation is performed on a semaphore.
(d) Interrupts must be disabled.
(e) None of the above is true.

Question 16. (5 points) Pre-emptive multiprogramming implies which one of the following:
(a) Critical sections (d) Re-entrant codes
(b) Unfair competition amongst resources (e) Interrupts
(c) Semaphores

Question 17. (5 points) When dealing with a simple multi-programming system, as described in class, what type of data structure holds process state information?
(a) A process control block (d) A ready queue
(b) A linked-list (e) A circular buffer
(c) None of these.

Question 18. (3 points) Of the following, which one does the processor hardware handle differently once it decides to service the condition?
(a) An Exception (b) A Trap (c) An Interrupt (d) A Reset (e) All are handled the same way.

Question 19. (5 points) A program must store a short sequence of stereo sound for playback. A left and right channel are used with a D-to-A converter to produce the sound. The D-to-A converter takes 16-bit input samples per channel to produce the analog voltage. The samples will be output at 44,000 Hz, to produce CD quality sound. Approximately how much storage does the program need to allocate to store 5 minutes of music?
(a) \( \sim 211.2 \text{ Mbytes} \) (b) \( \sim 52.8 \text{ Mbytes} \) (c) \( \sim 26.4 \text{ Mbytes} \) (d) \( \sim 880 \text{ Kbytes} \) (e) \( \sim 440 \text{ Kbytes} \)
Question 20. (3 points) A circular buffer would probably be used to implement:
(a) A ready queue
(b) A first-in first-out queue
(c) A data buffer
(d) a and c.
(e) b and c.

Question 21. (5 points) A system has four devices connected to it. Devices A and B are connected in a daisy chain to the level 4 priority line of a PIC, with A closer to the PIC than B. Devices C and D are connected to the level 5 priority line of the PIC, with C closer to the PIC. Assuming the interrupt service routines are properly written and everything is properly enabled, if all four devices simultaneously want to interrupt the CPU, what is the order in which the devices will be serviced? (Assume 68000 priority levels.)
(a) D, C, B, A
(b) A, B, C, D
(c) C, D, A, B
(d) C, A, D, B
(e) None of these.

Question 22. (5 points) Consider the following lines of code:
```
clr.w (A0)+
beq Label
```
How many machine cycles does it take to execute this code?
(a) 14
(b) 18
(c) 22
(d) 26
(e) Not enough information.

Some useful information.

Table D-1. Effective Address Calculation Times

<table>
<thead>
<tr>
<th>Addressing Mode</th>
<th>Byte Word</th>
<th>Long</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dn</td>
<td>0 (0/0)</td>
<td>0 (0/0)</td>
</tr>
<tr>
<td>An</td>
<td>0 (0/0)</td>
<td>0 (0/0)</td>
</tr>
<tr>
<td>(An)</td>
<td>4 (1/0)</td>
<td>8 (2/0)</td>
</tr>
<tr>
<td>(An)+</td>
<td>4 (1/0)</td>
<td>8 (2/0)</td>
</tr>
<tr>
<td>-(An)</td>
<td>6 (1/0)</td>
<td>10 (2/0)</td>
</tr>
<tr>
<td>d(An)</td>
<td>8 (2/0)</td>
<td>12 (3/0)</td>
</tr>
<tr>
<td>d(An,X)</td>
<td>10 (2/0)</td>
<td>14 (3/0)</td>
</tr>
<tr>
<td>xxx.W</td>
<td>8 (2/0)</td>
<td>12 (3/0)</td>
</tr>
<tr>
<td>xxx.L</td>
<td>12 (3/0)</td>
<td>16 (4/0)</td>
</tr>
<tr>
<td>d(PC)</td>
<td>8 (2/0)</td>
<td>12 (3/0)</td>
</tr>
<tr>
<td>d(PC,X)</td>
<td>10 (2/0)</td>
<td>14 (3/0)</td>
</tr>
<tr>
<td>#xxx</td>
<td>4 (1/0)</td>
<td>8 (2/0)</td>
</tr>
</tbody>
</table>

Table D-6. Single Instruction Execution Times.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Size</th>
<th>Register</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>Byte, Word</td>
<td>4 (1/0)</td>
<td>8 (1/1)+</td>
</tr>
<tr>
<td>Long</td>
<td>6 (1/0)</td>
<td>12 (1/2)+</td>
<td></td>
</tr>
</tbody>
</table>

+ add effective address calculation time

Table D-9. Conditional Instruction Execution Times.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Displacement</th>
<th>Branch Taken</th>
<th>Branch Not Taken</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bcc</td>
<td>Byte, Word</td>
<td>10 (2/0)</td>
<td>8 (1/0)</td>
</tr>
<tr>
<td>BRA</td>
<td>Byte, Word</td>
<td>10 (2/0)</td>
<td>-</td>
</tr>
<tr>
<td>BSR</td>
<td>Byte, Word</td>
<td>18 (2/0)</td>
<td>-</td>
</tr>
<tr>
<td>DBcc</td>
<td>CC true, CC false</td>
<td>10 (2/0)</td>
<td>12 (2/0)</td>
</tr>
</tbody>
</table>