1. The 8086 instruction set includes two instructions, RET and IRET. Which one of the following statements is true about these two instructions?

   a. They can be used interchangeably.
   b. RET is used to return from a near call, IRET is used to return from a far call.
   c. IRET restores the flags register, RET does not.
   d. IRET sets IF.
   e. RET sets IF.

2. Which one of the following statements is true about the interrupt type code:

   a. It is the address of the interrupt handler.
   b. It is only used in hardware interrupts.
   c. It is used to flag improper use of data types.
   d. It converts from BCD to binary.
   e. None of the above.

3. Which one of the following statements is true about a type 5 interrupt:

   a. It is generated when the wrong data type is used in an arithmetic instruction.
   b. It has a handler whose far pointer is located at address 20.
   c. It will be generated when an attempt is made to divide by zero.
   d. It is of the class of software-only interrupts.
   e. None of the above.

4. Which one of the following statements about interrupt handlers is true:

   a. The handler can be invoked by hardware or software.
   b. The handler is a procedure call.
c. Handlers must disable interrupts.
d. Handlers need to save only registers used by their caller.
e. All of the above.

The following four questions concern an asynchronous serial communications channel operating at 4800 Baud. The protocol specifies one start bit, 7 data bits, odd parity, and one stop bit. A “mark” is represented as a 1.

5. The frame that represents the transmission of “+” is (the hexadecimal representation of “+” is 2BH).
   a. 01101010011   b. 1110101010   c. 0010101111   d. 0101101011
   e. 0110101011

6. The maximum number of characters that can be transmitted in one second over this channel is:
   a. 436   b. 480   c.686   d. 4800   e. None of these.

7. The time to transmit a single bit over this channel is:
   a. 208 microseconds.   b. 4800 microseconds. c. 480 microseconds. d. 2.8 milliseconds.
e. 4.8 microseconds.

8. Assume that a character received over this channel is placed in AL, including the parity bit. The validity can be checked and the parity bit removed by the code:

   a. AND AL, 7FH
   JPE BAD
   AND AL, 80H
   b. TEST AL, 7FH
   JPE BAD
   AND AL, 80H
   c. TEST AL, AL
   JPE BAD
   AND AL, 7FH
   d. TEST AL, AL
   JPE BAD
   OR AL, 00H.
e. None of the above.
9. Suppose you wished to clock a Digital to Analog converter once every 1/10th second, and you must generate the clocking signal from a 24-bit counter-timer that is itself clocked by a 2 MHz clock. You should initialize the counter-timer with the following (decimal) value:
   a. $2 \times 10^6$   b. $2 \times 10^5$   c. $5 \times 10^4$   d. $5 \times 10^3$   e. $2^{24}$.

10. What is the period of a 400 MHz clock?
   a. 4 ns. b. 4 microseconds. c. 2.5 ns. d. 2.5 microseconds. e. None of these.

11. A compact disk stores a sequence of 16-bit values representing left and right channels of music, each sampled at 44 KHz. How many bytes will be required to store a 10 minute song?
   a. ~106 MB. b. ~10 MB c. ~50MB d. ~101 MB e. ~1.6 GB.

12. An 8-bit Digital to Analog converter has a range from 0 to 10 volts. What is the maximum error that it will make if all errors are due to quantization?
   a. 195 mV. b. 390 mV. c. 19.5 mV. d. 39 mV. e. 25.6 mV.

13. Which one of the following statements is true about a critical section:
   a. It cannot use re-entrant code.
   b. It cannot be interrupted without destroying its correctness.
   c. It must use a semaphore to make it correct.
   d. It is one whose correctness can be interfered with by another process or program.
   e. It is critical because the programmer will be fired if it is incorrect.
14. Pick the single best answer from the following list: In order to be re-entrant a program must:

a. Have multiple data segments.
b. Be recursive.
c. Have separate data storage for each process that uses it.
d. Have a separate code space for each user or process.
e. Be recursive and have separate code space for each user or process.

15. Which single statement of from the following list is true? In DMA transfers:

a. Cycle stealing is implemented by interrupts.
b. Blocks are transferred by interrupts.
c. Interrupts must be disabled unless cycle stealing is implemented.
d. The DMA device must be bus master during data transfers.
e. The DMA controller transfers data from an external device to the CPU.

16. Preemptive scheduling implies which one of the following:

a. Critical sections
b. Unfair competition amongst resources.
c. Semaphores.
d. Re-entrant code.
e. Interrupts.

17. Which one of the following statements is true about the Intel 8086 IN and OUT instructions:

a. They access memory and peripheral devices.
b. They were devised to increase address space.
c. They must be used with handshaking.
d. They can be used in place of MOV instructions.
e. They are used to transfer data from Input devices to Output devices.