1. (4 points) In the space below, calculate the 8-bit 2’s complement representation of the decimal value -20. Express your answer in binary. Show your work. No partial credit.

2. (10 points) Convert the following C conditional statement to 8086 assembly language. Assume all variables have been properly defined in a data segment, all segments have been properly initialized, and other boilerplate code is present. That is, only provide code for the statement below.

```c
if (A <> B) A = B;
```

3. (4 points) Given the following state of an 8086: IP = 00FFH, CS = 2000H, DS = 3000H, SS = 6000H, ES = 9000H. From what physical address will the next instruction be fetched? Show your calculations, and show your answer in hexadecimal. No partial credit.

4. (9 points) Convert the decimal value -1.25 to an IEEE 32-bit real. Show your work, show your answer in binary, and indicate the sizes and bit locations of the important fields.

5a. (7 points) Draw a figure showing an RS232 frame with one start bit, 7 data bits, a parity bit, and one stop bit. Indicate the mark and space binary values and lsb and msb locations.
5b. (6 points) How many ASCII characters can be sent in one second over a serial data transmission channel using the frame above if the data transmission rate is 28,800 bits per second. Show your calculations. No partial credit.

6. (5 points) A user wishes to employ an 8-bit, 10 volt full-scale ADC to sample a laboratory experiment. The user wishes to be able to distinguish voltage differences of 10 millivolts. Will the ADC described above be appropriate for the user's needs? Show your work to prove your answer.

7. (5 points) In order for a DMA controller to operate it must become bus master. Draw in the space below a figure showing and naming the two signals that it and the CPU use in order to establish and relinquish control of the bus. Also show on the figure the direction in which each of the signals travels.

8. (5 points) What particular mechanism does an 8086 programmer employ to control whether or not hardware interrupts are recognized? This question refers to the 8086 CPU and its registers and instructions, not peripheral devices. Be specific about register bit names, and opcodes.

9. (4 points) At what decimal physical address will the vector for a type 10 (decimal) interrupt be found? Show your calculations. No partial credit.
10. (8 points) Why is the LOCK prefix needed before an instruction `XCHG A, Sem`, that will be used to test and set the value of a semaphore?

11. (7 points) When a DMA controller is being used, what is the purpose of the cycle-stealing mode? Answer in one or two sentences.

12. (10 points) Draw in the space below the mechanism by which BASE and LIMIT registers are used to provide memory management and protection (not virtual memory, just memory management and protection). Show the incoming EA, how the BASE and LIMIT registers are used, and the location in physical memory where the addressed value will be found.

13. (5 points) Given the macro

```assembly
DecBytes MACRO A, B, Symbol
Symbol DB A DUP (B) ; A copies of B
ENDM
```

If the assembly language programmer types

```assembly
DecBytes Stuff 100 ‘ABCDE’
```

show what the expanded macro will look like, in the space below.
14. (4 points) What is the period of a 400 MHz clock? Show your work. Indicate the units that you have expressed the answer is in. No partial credit.

15. (12 points) Consider a 2-way set associative cache with 64-byte lines. The processor issues 32-bit addresses. The cache is 64 K bytes in size. Fill in the sizes (not the bit numbers) of the TAG, INDEX, and OFFSET fields in a 32-bit memory reference. 4 points for each correct field.

<table>
<thead>
<tr>
<th></th>
<th>TAG</th>
<th>INDEX</th>
<th>OFFSET</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

16. (5 points) Explain in one or two sentences the specific purpose of the presence bit in virtual memory page table entries.

17. (2 points each) Answer T, True or F, False to each of the following questions:

The cache mapping function is implemented in software________.

There will be a “dirty bit” associated with virtual memory pages in main memory____.

DMA can be used to speed virtual memory paging______.

An 8-way set-associative cache will be 8 times faster than a directed mapped cache____.

Superscalar architectures are used primarily for calculations involving scaling____.