Active device operation, pspice simulation

Download the “mos.lib” library file from the course notes (see comments in header). Run SPICE simulations (using Orcad in labs or any other variant of SPICE) for the following subparts, using either netlist files or schematic capture (for netlist, include library with an “inc mos.lib” statement). See the online PSPICE manual for description of the BSIM3v3.1 model (level 7) and the non-idealities included. Note that the SPICE nmos Level 1 model is very similar to the approximate hand calculation equations we are using in class (see online manual for equations). The SPICE BSIM3v3.1 model (level 7 in Orcad) is based on physical characteristics which include many non-idealities (you should read brief description in the online manual).

The purpose of this exercise is to gain experience simulating active devices in SPICE and to gain intuition on the relative accuracy of our simplified hand calculations and the range of operating conditions where we can expect them to be good approximations.

a) nmos characteristics: refer to the figure below, with device width and length values shown (in um). For simulation, use the “n” level 1 model for M1 and the “nbsim” BSIM3 version 3.1 model for Mbsim.

1. Perform a DC sweep on Vgs from 0V to 5V with Vds = 3V. Turn in one plot with I1 and Ibsim vs Vgs. Note the range of drain currents where the simple Level 1 model is accurate. Also, zoom in on the drain current near the threshold voltage and note differences between the models.

2. Perform a DC sweep on Vds from 0V to 8V with Vgs = 1.5V. Turn in one plot with I1 and Ibsim vs Vds. Note the range of drain currents and voltages where the simple Level 1 model is accurate. Repeat the simulation at different device lengths and Vgs values and comment on the simple level 1 model accuracy (only comment, no additional plots required).

![nmos circuit diagram](image)

b) pmos characteristics: repeat part a) for pmos devices, using same W/L dimensions, Vsod = 3V (for Vgs sweep) and Vsg = 2V (for Vsd sweep).

c) current mirror: refer to the figure below, with device width and length values shown (in um). For simulation, use “n”level 1 model for M1 & M2 and “nbsim” BSIM3 model for M1b & M2b.

1. Perform a DC sweep of Vo from 0V to 8V. Turn in a single plot of I2 and I2b vs Vo. Comment on the differences between Level 1 & BSIM models

2. Repeat DC sweep of Vo from 0V to 8V, but use M2b with “W=2u L=2u m=10”, which uses the “m” parameter to model paralleled devices. Turn in a single plot of I2 & I2b vs Vo. Note significantly better matching in the BSIM version. This is due to inclusion of layout mismatch (due to lithography) errors in the BSIM model. Significantly better matching is achieved when paralleling identical devices.

![current mirror circuit diagram](image)