ECEN 5008: Analog IC Design

Midterm Exam #1, Fall 2004

Instructions:

1. Exam Policy:
   • Time limited, 50 minute exam. When the time is called, all work must stop. **Put your initials on the top of each page before the exam ends.**
   • Closed book. One 8.5" x 11" note sheet is allowed. No cooperation is allowed.
   • Show all work, partial credit will be given.

2. **Work in the space provided**, or on the back of the sheet, if necessary. Turn in these sheets.

3. The exam has 2 problems. The maximum number of points for each question and part is indicated in the square brackets. Note that each part can be solved independently – **attempt ALL parts!**

______________________________
NAME:

Problem 1 [54]:

Problem 2 [46]:

TOTAL [100]:

© 2004, R.Zane, University of Colorado at Boulder
1. **[54 points]** In the CMOS circuit of Figure 1, the device parameters are as follows:

**NMOS:** \(\mu_n C_{ox} = 100 \mu A/V^2, V_{tn} = 1 V, \gamma_n \approx 0, \lambda_n \approx 0\)

**PMOS:** \(\mu_p C_{ox} = 50 \mu A/V^2, |\gamma_p| = 1 V, \gamma_p \approx 0, \lambda_p \approx 0\)

The device aspect ratios \(W/L\) in \(\mu m/\mu m\) are shown in the figure. Note that M4 is PMOS and M3 is NMOS. For each part, show your work in the space provided and repeat your solution neatly in the box provided.

(a) **[16]** For the DC input \(V_{ii} = 7 V\), solve for the DC input voltage \(V_{ii}\) such that the DC output voltage is forced to \(V_o = 5 V\). At this operating point, state the operating mode of each device and label the currents \(I_1\) through \(I_3\).

\[
\begin{align*}
V_{ii} &= \quad \text{M1:} \\
I_1 &= \quad \text{M2:} \\
I_2 &= \quad \text{M3:} \\
I_3 &= \quad \text{M4:}
\end{align*}
\]
(b) [12] For the DC input voltages shown in the table below, fill in the operating modes of each device (C, A, or T) with the following notation: C: Cutoff, A: Active/sat, T: Triode

<table>
<thead>
<tr>
<th>$V_{i1}$</th>
<th>$V_{i2}$</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
</tr>
</thead>
<tbody>
<tr>
<td>10V</td>
<td>10V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7V</td>
<td>0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0V</td>
<td>0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(c) [16] At the DC operating point $V_{i1} = 8V$, $V_{i2} = 7V$, solve for the small-signal gain $v_o/v_{i1}$ and output resistance $R_{out}$. Give analytical expressions in terms of small-signal parameters and numerical values. Note that input #2 is DC for this part.

(expression): $A_{i1} = \frac{v_o}{v_{i1}} = \ldots$

(expression): $R_{out} = \ldots$

(numerical): $A_{i1} = \frac{v_o}{v_{i1}} = \ldots$

(numerical): $R_{out} = \ldots$
(d) [10] At the DC operating point $V_{i1} = 8V$, $V_{i2} = 7V$, solve for the small-signal gain $v_o/v_{i2}$. Note that input #1 is DC for this part.

(expression): $A_{r2} = \frac{v_o}{v_{i2}}$

(numeralical): $A_{r2} = \frac{v_o}{v_{i2}}$
2. [46 points] In the current reference circuit of Figure 2, the device parameters are as follows:

\[ \mu_n C_{ox} \approx 100 \mu A/V^2, \quad V_m \approx 1V, \quad \gamma \approx 0, \quad \lambda_n \approx 0 \]

\[ \mu_p C_{ox} \approx 50 \mu A/V^2, \quad V_{tp} \approx 1V, \quad \gamma \approx 0, \quad \lambda_p \approx 0 \]

The MOS device aspect ratios \( W/L \) in \( \mu m/\mu m \) are shown. For each part, show your work in the space provided and repeat your solution neatly in the box provided.

![Figure 2: Current reference circuit for Problem 2.](image-url)

(a) [18] Write an expression for the bias current \( I_b \) as a function of device parameters and the bias resistor \( R_b \), then solve for the bias resistor required to achieve \( I_b = 10 \mu A \). You can assume that all currents are greater than zero. You must show your work to receive any credit on this part.

(expression): \( I_b = \)

(numerical): \( R_b = \)
(b) [10] Draw a suitable bootstrap circuit to force the reference of Fig. 2 out of the zero current operating point without affecting normal operation. You can use the space on the back of the opposite page for your work if needed, but re-draw your complete solution neatly directly on Fig. 2. Describe below in one or two sentences or expressions how your bootstrap circuit works at startup & normal operation.

*Startup:*

*Normal Op:*

(c) [6] Although channel length modulation has been neglected in this problem, it will cause the power supply sensitivity to be non-zero for the circuit in Fig. 2. Draw in the space below a modified circuit from Fig. 2 that will have improved power supply sensitivity using only two additional devices (nmos or pmos). You do not have to calculate the sensitivity, just draw the circuit schematic and give one sentence describing why the sensitivity is improved. You do not need a bootstrap circuit for this part.
(d) [12] For this part, you can assume that the current $I_1$ in Fig. 2 is given by the following expression:

$$I_1 = \frac{4}{R_5 K_4}, \quad \text{where} \quad K_4 = \frac{\mu_p C_{ox} W_4}{2 L_4}$$

Solve for the fractional temperature coefficient of the current $I_1$. In the box below, write an expression for the fractional temperature coefficient in terms of process parameter fractional temperature coefficients, then write the numerical solution. The coefficients for key process parameters are given below. *Note: you only need two of the three parameters given below.*

Transconductance: $k_p' = \mu_p C_{ox}$, $TC_F(k_p') = \frac{1}{k_p'} \frac{\partial k_p'}{\partial T} = -4000 \text{ ppm/}^\circ\text{C} = -4.0 \cdot 10^{-3} /^\circ\text{C}$

Threshold: $TC_F(V_t) = -3000 \text{ ppm/}^\circ\text{C} = -3.0 \cdot 10^{-3} /^\circ\text{C}$

Resistor: $TC_F(R) = \frac{1}{R} \frac{\partial R}{\partial T} = -1200 \text{ ppm/}^\circ\text{C} = -1.2 \cdot 10^{-3} /^\circ\text{C}$

(expression): $TC_F(I_1) =$

(numerical): $TC_F(I_1) =$