Design an op-amp to meet the following specifications given the constraints and process parameters listed below. You should use hand-calculations for an initial op-amp design, then perform spice (using Orcad or unix Spice) simulations and any iterations necessary to meet the specifications. Turn in the work requested below, in the order specified. You do not have to layout the circuit in Magic.

**Op-Amp Specifications:**
- The following specs are for a 0V to 2V 1MHz square-wave input signal, with the op-amp configured as a unity-gain non-inverting voltage buffer:
- Common-mode input voltage range and output voltage range sufficient to follow the input signal.
- Design for 90% rise-time \( \approx 2.5\tau = 50\text{ns} \), where \( \tau = \frac{1}{2\pi(BW)} \), and BW = Bandwidth of the closed-loop system.
- No output signal overshoot.
- No output slew-rate (SR) limiting behavior.
- Output must drive a load resistance of \( R_{\text{load}} = 1k\Omega \).
- Min open-loop low-frequency gain: \( A_{o,OL} \geq 10,000 \).

**Constraints:**
- The supply voltages are VDD = +5V and GND = 0V.
- One ideal current source is available for DC biasing.
- One resistor and capacitor are available for compensation, if desired.
- Min overdrive for all devices is \( V_{od} = |V_{GS}| - |V_{i}| \geq 0.15V \).
- Assume a poly-poly capacitor when calculating area required for compensation capacitor.

**Process Parameters:**
- The device parameters are as shown in the spice models below:
  - .model nm nmos kp=60u vto=0.7 lambda=**** tox=25nm
cgs=0.18nF cgdo=0.18nF cbs=100fF cbd=100fF mj=0.5 pb=0.65
  - .model pm pmos kp=30u vto=-0.9 lambda=**** tox=25nm
cgs=0.26nF cgdo=0.26nF cbs=200fF cbd=200fF mj=0.5 pb=0.65
  - **** where lambda is a function of device length, and a separate .model statement should be used for each device length used:
    - Lambda_nmos = 0.12 / L, with L=device length in um
    - Lambda_pmos = 0.06 / L, with L=device length in um
- Capacitances:
  1. Gate-to-Source (cgs above is nF/m, vs Cox below is fF/um^2):
2. Gate-to-Drain:
\[ C_{gd} = W \cdot CGDO \]

3. Source and drain to substrate (estimation, removes requirement to calculate area and perimeter of source and drain depletion regions):
\[
\begin{align*}
C_{sb} &= \frac{CBS}{(1 + V_{SB}/PB)^{MJ}} \\
C_{db} &= \frac{CBD}{(1 + V_{DB}/PB)^{MJ}}
\end{align*}
\]

4. Gate oxide capacitance: \( C_{ox} = 0.16 \text{ fF/\mu m}^2 \)

5. Poly-Poly capacitance: \( C_{ox} = 0.57 \text{ fF/\mu m}^2 \)

• MIN device length and width = 2um; assume that the layout would be performed on a 0.1um grid (not the lambda grid we’ve used in the past).

**Turn-In (in the following order):**

• Complete schematic of your op-amp with labeled device sizes, bias current, and capacitor size.

• Table of the final op-amp specifications (after simulation & iteration), including:
  o Open-Loop: Common-mode input voltage range, output voltage range, low-frequency gain, gain-BW product, slew-rate limit, and output current drive limits.
  o Closed-Loop: unity-gain system BW and Phase Margin.

• Table showing total device W*L area and compensation poly-poly capacitor area (extra-credit for design with minimum area), and total quiescent power consumption (with Vi=Vo=0V).

• Spice simulations to show that the op-amp specs have been met.

• Hand calculations that show how you designed the op-amp.