Figure below show the basic CMOS logic inverter gate used to drive capacitive load $C_L = 1\, \text{pF}$. All other capacitances can be neglected. The supply voltage is $V_{DD} = 5\, \text{V}$. The device Spice models are:

```
.model nm nmos kp=60u vto=1 lambda=0 gamma=0
.model pm pmos kp=20u vto=-1 lambda=0 gamma=0
```

Note that the Spice parameter $kp$ is equal to $\mu_n C_{ox}$ for NMOS or $\mu_p C_{ox}$ for PMOS devices.

All devices have the same channel length $L_1 = L_2 = L = 1\,\mu\text{m}$.

(a) Design the inverter, i.e., find the device channel widths $W_1, W_2$, so that the inverter propagation delays are $t_{df} = t_{dr} = 1\,\text{ns}$. You can assume that the rise and the fall times of the input pulse are very short.

(b) Verify your design in (a) using Spice simulation with the input pulse:

```
vi in 0 pulse 0 5 0 1n 1n 5n 10n
```

Using the simulation result for $v_i(t)$ and $v_o(t)$, find $t_{df}, t_{dr}, t_f, t_r$ with $W_1, W_2$ from part (a). Then, if necessary, modify $W_1, W_2$ to meet the specs for $t_{df}, t_{dr}$.

![Figure 1: CMOS inverter gate with Spice models and input pulse](image-url)