Figure below show a clocked voltage comparator using two CMOS logic inverters. The devices sizes in \( \mu m/\mu m \) are indicated in the figure. The supply voltage is \( V_{DD} = 5V \). \( C_1 = 0.1pF, C_2 = 0.2pF \) are combined device capacitances, \( C_3 = 1pF \) is added to eliminate the comparator offset, and \( C_4 = 1pF \) is the capacitive load at the output of the comparator. All other capacitances can be neglected.

The device Spice models are:

```
.model nm nmos kp=60u vto=1 lambda=0 gamma=0
.model pm pmos kp=30u vto=-1 lambda=0 gamma=0
```

Note that the Spice parameter \( kp \) is equal to \( \mu_n C_{ox} \) for NMOS or \( \mu_p C_{ox} \) for PMOS devices.

The clock signals \( \phi_1, \phi_2 \) are 0 to \( V_{DD} \) pulses with period \( T = 1\mu s \) and \( t_{ON} = 0.45\mu s \) as shown in the figure.

Output of the comparator is valid at the end of the \( \phi_2 \) on interval. At this time, ideally, \( v_o = +V_{DD} \) if \( v_i > 0 \), and \( v_o = 0 \) if \( v_i < 0 \).

(a) Find, sketch and label waveforms \( v_1(t), v_o(t) \) during one period of the clock for two input voltages:

(1) \( v_i = +0.1V \) and (2) \( v_i = -0.1V \). You can assume very short rise and fall times of the clocks and at the inverter outputs. On the waveforms indicate how operating modes of the devices change in time.

(b) Verify the results in (a) using Spice simulation using the clocks:

```
vp1 phi1 0 pulse 0 5 0 1n 1n 0.45u 1u
vp2 phi2 0 pulse 0 5 0.5u 1n 1n 0.45u 1u
```

Turn in the corresponding waveforms obtained by simulation and comment on differences with respect to the theoretical plots.

(c) Repeat the simulations in (b) with the device parameters \( kp, vto \) changed by \( \pm 10\% \) (you can make the \( +10\% \) or \( -10\% \) changes as you wish). Does the comparator still give the correct output at the end of the \( \phi_2 \) on interval?