Op-amps used in the SC integrators in this problem can be considered ideal, except that the output voltage cannot exceed the supplies: \( V_{O_{\text{max}}} = V_{DD} = +5\text{V}, \) and \( V_{O_{\text{min}}} = V_{SS} = -5\text{V}. \)

(a) Sketch an inverting, parasitic-insensitive SC integrator. Assuming that signal frequencies are much smaller than the clock frequency \( f_s \), pick capacitance values (relative to value \( C \)) so that the approximate transfer function of the integrator is \( H(s) = -4f_s/s \). Write \( H(z) \) for this SC integrator.

(b) For the input shown in Figure (a), find, sketch and label the output \( v_o(t) \) in Fig.(a) for the SC integrator of part (a). Initially, \( v_o(0) = 0 \).

Figure (b) shows another SC integrator.

(c) Assuming that signal frequencies are much smaller than the clock frequency \( f_s \), find the approximate \( H(s) = v_o/v_i \) of the SC integrator in Figure (b). Hint: find the charge \( \Delta Q \) delivered to the feedback capacitor over a clock period \( T \), and the equivalent resistance \( R_{eq} \) of the SC network between the input and the virtual ground.

(d) Is the SC integrator of Figure (b) parasitic insensitive? Justify your answer.

(e) Given the input shown in Figure (a), find, sketch and label \( v_o(t) \) in Fig.(a) for the SC integrator of Figure (b). Initially, \( v_o(0) = 0 \).

(f) Find \( H(z) = v_o/v_i \) for the SC integrator shown in Figure (b).
Inverting parasitic-insensitive SC integrator

SC integrator of Fig. (b)