The purpose of this problem is to examine layout of a basic op-amp configuration shown in Figure 1, and to see an example of layout techniques that are frequently used to improve performance of analog circuits.

Layout of a device $M_i$ with a large aspect ratio $W_i/L_i$ is usually done by combining several ($n_i$) devices with smaller aspect ratio $W'/L_i$ in parallel, so that $n_i W' = W_i$. The drain and source areas are shared between adjacent paralleled devices. This technique is applied to the devices $M_6$ and $M_{10}$ in the circuit diagram. Advantages of this layout include: (1) smaller total area and more convenient shape compared to a long, flat layout; (2) smaller source and drain junction capacitances and contact resistances because the drain/source areas of the adjacent paralleled devices are shared.

The layout technique where a device consists of a parallel connection of several smaller devices also improves accuracy of scale factors in structures such as current mirrors and differential amplifiers. For example, consider a mirror with devices $M_i$ and $M_j$, where $W_i/L_i = n_i W'/L$ and $W_j/L_j = n_j W'/L$. Second-order effects in the fabrication process cause errors $\Delta W$ and $\Delta L$ in the resulting fabricated device sizes. However, if these errors are approximately the same for all devices, the mirror current ratio is still precisely determined by the integer ratio $n_i/n_j$. For example, this technique is applied to the mirror consisting of $M_7$, $M_8$ and $M_9$ devices in the circuit diagram. Furthermore, it is possible to interleave smaller ($W'/L$) devices in order to minimize the effects of variations in device parameters across the die. In particular, interleaving is commonly applied in layout of differential pairs (such as $M_1$, $M_2$ in the circuit diagram) to improve matching and minimize offset.

The opamp layout includes a parallel-place capacitor $C_c$ where the bottom plate is the poly layer and the top plate is the second poly layer called poly2 or electrodecap layer. The metal1 to poly2 contact is called p2c.

Copy the file opamp1.mag to your folder and start magic using:

```
prompt> cp ~maksimov/4228/opamp1.mag .
prompt> magic -T scna.60 opamp1
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a) Examine the layout and for each device find the number $n_i$ of the devices connected in parallel, and the aspect ratio $W_i'/L_i$ in $\mu m/\mu m$ of each paralleled device. Also find the total device aspect ratio $W_i/L_i$. Put your results in a table (no credit will be given otherwise).

b) Find the area of the electrodecap layer used to construct $C_c$, and find the capacitance $C_c$ if the poly to electrodecap capacitance per unit area is $0.6 fF/\mu m^2$.

You may find the following magic commands useful:

- If you point the mouse cursor over a layer and press "s" ("select") repeatedly, all electrically connected layers will be eventually selected. This can be used to check electrical connections in a layout.
- If you point the mouse cursor to a layer and select the layers (using "s" or other selection commands), the command :what returns the names of the selected layer in the text window.
- The command :box returns the box size (in lambda) in the text window. Lambda is equal to $0.6 \mu m$ in the scna.60 technology.