2.26, Consider the C int array variable V[2]. Assume that C ints are 32 bits in size and that the base address of V is in r3.

Write a single SRC instruction similar to those in Exercise 2.25 that will store V[2] in r4.  

\( \text{Solution:} \) The SRC instruction to store V[2] is:  
\[
\text{load r4, 8[r3]}
\]

2.27b. Using the hardware in Figure 2.24, write the RTN description and the control sequence that implements the following:


\( \text{(§2.6)} \)

Draw timing diagrams similar to Figure 2.25 for the control sequences developed above.  

\( \text{(§2.6)} \)

\( \text{Solution:} \)

\[
\begin{array}{c|c}
\text{b.} & \text{Y } \leftarrow \text{ R[6];} & \text{R[6]}_{\text{out}}, \text{Y}_{\text{in}}; \\
& \text{Z } \leftarrow \text{ R[5] + Y;} & \text{R[5]}_{\text{out}}, \text{Z}_{\text{in}}; \\
& \text{Y } \leftarrow \text{ Z;} & \text{Z}_{\text{out}}, \text{Y}_{\text{in}}; \\
& \text{Z } \leftarrow \text{ R[4] + Y;} & \text{R[4]}_{\text{out}}, \text{Z}_{\text{in}}; \\
& \text{R[3] } \leftarrow \text{ Z;} & \text{Z}_{\text{out}}, \text{R[3]}_{\text{in}}; \\
\end{array}
\]