More about the zero-voltage switching boundary

(of the active-clamped forward converter)

The resonant transition associated with the turn off of $Q_1$ and the turn on of $Q_2$ is relatively easy:

The positive $i_m$ plus the positive reflected load current ($i_L$) both combine to charge $v_{ds}$ up to $V_g + V_b$. Partway through this transition, $D_3$ becomes reverse-biased and $i_L$ is zero; if $v_{ds}$ is not yet charged up to $(V_g + V_b)$ at this point, then enough magnetizing current must be left to finish the job. Nonetheless, this is the easier ZVS transition.

The resonant transition associated with the turn off of $Q_2$ and the turn on of $Q_1$ normally requires more energy stored in $i_m$.

At the beginning of this transition, $D_3$ is reverse-biased and $i_L = 0$. The negative magnetizing current in $D_3$ discharges $v_{ds}$ from $(V_g + V_b)$ to $V_g$ (subinterval 6). Diode $D_3$ then becomes forward-biased and the load current begins shifting from $D_4$ (during subinterval 7).
to $D_3$. At the same time, $i_m$ continues to discharge $C_{as}$ and $V_{ds}$. Note that, although $i_m(t)$ is negative, the reflected $i_C(t)$ is positive. For ZVS to occur, the magnitude of the negative $i_m(t)$ must be greater than the reflected load current for the entire time needed to discharge $V_{ds}$ to zero and for the gate driver to turn on $Q_1$. Note that a reduced transformer coupling coefficient, which implies larger $L_e$ and smaller $L_M$, tend to help this process. Indeed, a large $L_e$ allows the magnetizing current to discharge $C_{as}$ with minimal need to overcome the reflected load current; as usual, the disadvantage of this is the corresponding reduction in effective duty cycle caused by the increase in the length of subinterval $t$.