This assignment should be completed by Wednesday, October 4th. Note: there is nothing to hand in for this assignment. In this homework assignment, you will explore:

- Timing
- Logic Analyzers
- I/O ports
- Course web site
- Memory

The assigned reading will be available on the course web site in PDF format.

1. Read the handout from class "Understanding Timing Diagrams and the C501 Data Sheet". 
2. Why are the setup and hold times for chips important? 
3. Suppose you're examining the interface between a processor and an EPROM.
   a) Why is the access time of the EPROM important?
   b) Why is the float time of the EPROM important?
   c) What is bus contention or "drive fight"?
4. Read Agilent Application Note 1337 "Feeling Comfortable with Logic Analyzers", available on the course web site (or from http://www.agilent.com). 
5. Read the "Agilent/HP 1662A Logic Analyzer Notes" document available on the course web site. 
6. If you haven't completed your wire wrapping for Lab #2, finish that immediately, since Lab #2 is more time consuming than Lab #1. 
8. If you haven't done so already, go to the course web site and read the various pages in the Questions and Answers section.
9. [Optional] Review some of the Memory Technology links available on the course web site.