This assignment should be completed by Wednesday, February 15th. **Note: there is nothing to hand in for this assignment; however, you will use this memory map for Labs 2-4.** In this homework assignment, you will explore:

- Memory Maps, Glue Logic, Programmable Logic.

1. Design glue logic for your 8051 board which supports the following memory map: Your EPROM must be located starting at address 0000h and must occupy 24KB of address space (addresses 0000h-5FFFh). Note: The upper 8KB of the 32KB EPROM will not be used. Your SRAM must be located starting at address 6000h and must occupy 32KB of address space (addresses 6000h-DFFFh). The next 8KB of address space (addresses E000H-FFFFh) should be used for peripherals, which you will add later in the semester. Your decode logic should generate a chip select signal for the EPROM, a chip select for the SRAM, and a chip select for peripherals. Use a combined program and data space by ANDing the $PSEN$ and $RD$ lines to create a $READ$ signal. Options for your decode logic include discrete logic, a 74LS138, a 74LS156, or a PAL (if you know how to use PALs). Use a 74LS373 to demultiplex the 8051 address/data bus. If you choose to use a fast '245 transceiver to buffer Port 0, you can use the $READ$ signal to control the direction of data flow through the transceiver.

### Address in Binary | Hex | Address Use 
---|---|---
1111xxxxxxxxxxxxxx | FFFFh | Peripherals (8KB)
1110xxxxxxxxxxxxxx | E000h |
1101xxxxxxxxxxxxxx | DFFFh |
1100xxxxxxxxxxxxxx |
1011xxxxxxxxxxxxxx |
1010xxxxxxxxxxxxxx |
1001xxxxxxxxxxxxxx |
1000xxxxxxxxxxxxxx |
0111xxxxxxxxxxxxxx |
0110xxxxxxxxxxxxxx | 6000h |
0101xxxxxxxxxxxxxx | 5FFFh |
0100xxxxxxxxxxxxxx |
0011xxxxxxxxxxxxxx |
0010xxxxxxxxxxxxxx |
0001xxxxxxxxxxxxxx |
0000xxxxxxxxxxxxxx | 0000h |

2. **[Optional]** Visit the Lattice web site (http://www.latticesemiconductor.com/products/) and learn about GAL/PLD technology (see the GAL20V8 and ispGAL22V10) and CPLD technology. Visit the Xilinx web site (http://www.xilinx.com). Learn the basics of how the Xilinx FPGA technology works. Visit the web sites for Actel (http://www.actel.com) and Altera (http://www.altera.com), and understand how their technologies work.

3. **[Optional]** Search the Internet for web sites with good application notes or technology articles on at least two of the programmable logic technologies listed above. If you find any very good sites, send an e-mail message containing the URLs of these web sites along with a one or two sentence clearly-written synopsis of each web site to your instructor at Linden.McClure@Colorado.EDU. The URLs should be fully qualified: use http:// in each URL, so that one can click on the URL in your e-mail to go immediately to that web site.