Derivation of the flyback converter

The flyback converter is based on the buck-boost converter. Its derivation is illustrated in Fig. 1. Figure 1(a) depicts the basic buck-boost converter, with the switch realized using a MOSFET and diode. In Fig. 1(b), the inductor winding is constructed using two wires, with a 1:1 turns ratio. The basic function of the inductor is unchanged, and the parallel windings are equivalent to a single winding constructed of larger wire. In Fig. 1(c), the connections between the two windings are broken. One winding is used while the transistor $Q_1$ conducts, while the other winding is used when diode $D_1$ conducts. The total current in the two windings is unchanged from the circuit of Fig. 1(b); however, the

![Diagram of flyback converter derivation](image)

**Fig. 1.** Derivation of the flyback converter: (a) buck-boost converter, (b) inductor $L$ is wound with two parallel wires, (c) inductor windings are isolated, leading to the flyback converter, (d) with a $1:n$ turns ratio and positive output.
current is now distributed between the windings differently. The magnetic fields inside the inductor in both cases are identical. Although the two-winding magnetic device is represented using the same symbol as the transformer, a more descriptive name is “two-winding inductor”. This device is sometimes also called a “flyback transformer”. Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer. Figure 1(d) illustrates the usual configuration of the flyback converter. The MOSFET source is connected to the primary-side ground, simplifying the gate drive circuit. The transformer polarity marks are reversed, to obtain a positive output voltage. A $1:n$ turns ratio is introduced; this allows better converter optimization.

**Analysis of the flyback converter**

The behavior of most transformer-isolated converters can be adequately understood by modeling the physical transformer with a simple equivalent circuit consisting of an ideal transformer in parallel with the magnetizing inductance. The magnetizing inductance must then follow all of the usual rules for inductors; in particular, volt-second balance must hold when the circuit operates in steady-state. This implies that the average voltage applied across every winding of the transformer must be zero.

Let us replace the transformer of Fig. 1(d) with the equivalent circuit described above. The circuit of Fig. 2(a) is then obtained. The magnetizing inductance $L_M$ functions in the same manner as inductor $L$ of the original buck-boost converter of Fig. 1(a). When transistor $Q_1$ conducts, energy from the dc source $V_s$ is stored in $L_M$. When diode $D_1$ conducts, this stored energy is transferred to the load, with the inductor voltage and current scaled according to the $1:n$ turns ratio.

![Flyback converter circuit](image)
During subinterval 1, while transistor Q1 conducts, the converter circuit model reduces to Fig. 2(b). The inductor voltage \( v_L \), capacitor current \( i_C \), and dc source current \( i_g \), are given by

\[
\begin{align*}
    v_L &= V_g \\
    i_C &= -\frac{V}{R} \\
    i_g &= i \\
\end{align*}
\]

With the assumption that the converter operates with small inductor current ripple and small capacitor voltage ripple, the magnetizing current \( i \) and output capacitor voltage \( v \) can be approximated by their dc components, \( I \) and \( V \), respectively. Equation (1) then becomes

\[
\begin{align*}
    v_L &= V_g \\
    i_C &= -\frac{V}{R} \\
    i_g &= I \\
\end{align*}
\]  

(2)

During the second subinterval, the transistor is in the off-state, and the diode conducts. The equivalent circuit of Fig. 2(c) is obtained. The primary-side magnetizing inductance voltage \( v_L \), the capacitor current \( i_C \), and the dc source current \( i_g \), for this subinterval are:

\[
\begin{align*}
    v_L &= -\frac{V}{n} \\
    i_C &= \frac{I}{n} - \frac{V}{R} \\
    i_g &= 0 \\
\end{align*}
\]  

(3)

It is important to consistently define \( v_L(t) \) on the same side of the transformer for all subintervals. Upon making the small-ripple approximation, one obtains

\[
\begin{align*}
    v_L &= -\frac{V}{n} \\
    i_C &= \frac{I}{n} - \frac{V}{R} \\
    i_g &= 0 \\
\end{align*}
\]  

(4)

The \( v_L(t) \), \( i_C(t) \), and \( i_g(t) \) waveforms are sketched in Fig. 3.

Application of the principle of volt-second balance to the primary-side magnetizing inductance yields

\[
\begin{align*}
    \langle v_L \rangle &= D (V_g) + D' (-\frac{V}{n}) = 0 \\
\end{align*}
\]  

(5)

Fig. 3. Flyback converter waveforms, continuous conduction mode.
Solution for the conversion ratio then leads to

$$M(D) = \frac{V}{V_g} = n \frac{D}{D'}$$

(6)

So the conversion ratio of the flyback converter is similar to that of the buck-boost converter, but contains an added factor of \(n\).

Application of the principle of charge balance to the output capacitor \(C\) leads to

$$\langle i_C \rangle = D \left( -\frac{V}{R} \right) + D' \left( \frac{I}{R} - \frac{V}{R} \right) = 0$$

(7)

Solution for \(I\) yields

$$I = \frac{nV}{DYR}$$

(8)

This is the dc component of the magnetizing current, referred to the primary. The dc component of the source current \(i_g\) is

$$I_g = \langle i_g \rangle = D (I) + D' (0)$$

(9)

An equivalent circuit which models the dc components of the flyback converter waveforms can be constructed. The resulting dc equivalent circuit of the flyback converter is given in Fig. 4. It contains a 1:\(D\) buck-type conversion ratio, followed by a \((1 - D):1\) boost-type conversion ratio, and an added factor of 1:\(n\), arising from the flyback transformer turns ratio.

The flyback converter is commonly used at the 50-100W power range, as well as in high-voltage power supplies for televisions and computer monitors. It has the advantage of very low parts count. Multiple outputs can be obtained using a minimum number of parts: each additional output requires only an additional winding, diode, and capacitor. The peak transistor voltage is equal to the dc input voltage \(V_g\) plus the reflected load voltage \(V/n\); in practice, additional voltage is observed due to ringing associated with the transformer leakage inductance. A snubber circuit may be required to clamp the magnitude of this ringing voltage to a safe level that is within the peak voltage rating of the transistor.

Fig. 4. Flyback converter equivalent circuit model: (a) circuits corresponding to Eqs. (5), (7), and (9); (b) equivalent circuit containing ideal dc transformers.
Flyback transformer design

For this lab, you are given the following flyback transformer design tasks:

- select $L_m$ such that $\Delta i = 50\%$ of $I$
- use turns ratio $n = \frac{n_2}{n_1} = 1.5$
- use a PQ 32/20 core $\Rightarrow A_e, W_i, M_{LT}, L_m$ are given
- select turns $n_1$ such that total loss is minimized:
  \[
  \text{minimize } P_{tot} = P_{fe} + P_{cu}
  \]
- determine air gap length $h_g$
- determine primary and secondary wire gauges
- use fill factor $K_u = 0.4$
- check to make sure that the peak $B$ does not cause the core to saturate.

Choosing $n_1$ to minimize $P_{tot}$

We can relate $B_{ac}$ to $n_1$ and $\Delta i$ using the basic formula $\mathcal{A} = L_i$:

\[
B_{ac} = n_1 A_e B_{ac} = L_m \Delta i
\]

so $B_{ac} = \frac{L_m \Delta i}{n_1 A_e}$

Once we have solved the converter circuit to find the desired values of $L_m$ and $\Delta i$, then $L_m$, $\Delta i$, and $A_e$ are known. Hence this equation relates $B_{ac}$ to $n_1$. Increasing $n_1$ decreases $B_{ac}$, which decreases the core loss $P_{fe}$. 

5
Computing core loss

Core loss $P_{fe}$ depends on the peak value of the ac component of flux density $B_{ac}$. Manufacturers published data sheets contain plots of $P_{fe}$, that follow functions of the form

$$P_{fe} = K_{fe} B_{ac}^\beta A_{c \, lm}$$

see TDK H7C1 ferite data - course website links to data sheets

$K_{fe}$ is a constant of proportionality that depends on switching frequency and core material

$\beta$ is an exponent that depends on core material

$A_{c \, lm}$ is the volume of the core

For H7C1 material:

$\beta = 2.6$

$$K_{fe} = \begin{cases} 
16 & \text{at } 50 \text{ kHz} \\
40 & \text{at } 100 \text{ kHz}
\end{cases} \text{ at } 60^\circ \text{C}$$

with $A_{c \, lm}$ expressed in cm$^3$

$B_{ac}$ expressed in Tesla

$P_{fe}$ expressed in watts

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B-H loop caused by current ripple $ai$ in magnetizing current $i(t)$
Problem: increasing \( n_1 \) increases resistances of windings
\[ \Rightarrow \text{copper loss increases} \]

Resistance of windings

\[
\begin{align*}
\text{Primary winding area} & = \alpha_1 \frac{K w A}{n_1} \\
\text{Secondary winding area} & = \alpha_2 \frac{K w A}{n_2}
\end{align*}
\]

\[ \alpha_1 + \alpha_2 = 1 \]
\[ \alpha_1 = \text{fraction of } w A \text{ allocated to primary} \]
\[ \alpha_2 = \text{fraction of } w A \text{ allocated to secondary} \]

Wire areas

Primary wire area
\[ A_{w1} = \frac{\alpha_1 K w A}{n_1} \]
Secondary wire area
\[ A_{w2} = \frac{\alpha_2 K w A}{n_2} \]

Winding resistances

Primary winding resistance
\[ R_1 = \rho \frac{n_1 (H L L)}{A_{w1}} \]
Secondary winding resistance
\[ R_2 = \rho \frac{n_2 (N D L)}{A_{w2}} \]
Copper Loss

Primary winding copper loss: \( P_{Cu1} = I_{1,ms}^2 R_1 \)

Secondary winding copper loss: \( P_{Cu2} = I_{2,ms}^2 R_2 \)

Total copper loss: \( P_{Cu} = P_{Cu1} + P_{Cu2} \)

Note: carefully sketch the winding current waveforms \( i_1(t) \) and \( i_2(t) \), then compute their RMS values!

Copper loss vs. \( n_2 \):

\[
P_{Cu} = P_{Cu1} + P_{Cu2} = I_{1,ms}^2 R_1 + I_{2,ms}^2 R_2
\]

\[
= I_{1,ms}^2 \left( \frac{n_1}{\alpha_1 K_w A} \right) + I_{2,ms}^2 \left( \frac{n_1^2}{\alpha_2 K_w A} \right)
\]

\[
= \frac{\rho n_1^2 (MLT)}{K_w A} \left( \frac{I_{1,ms}^2}{\alpha_1} + \frac{n_1^2 I_{2,ms}^2}{\alpha_2} \right) \quad \text{with} \quad \alpha_2 = 1 - \alpha_1
\]

- Increasing \( n_2 \) increases copper loss.
- There is a value of \( n_2 \) that minimizes total loss.

Minimum copper loss occurs when window area is allocated as follows:

\[
\alpha_1 = \frac{I_{1,ms}}{I_{1,ms} + n I_{2,ms}} \quad \alpha_2 = \frac{n I_{2,ms}}{I_{1,ms} + n I_{2,ms}}
\]

A spreadsheet design approach:

- Choose \( \alpha_1 \) and \( \alpha_2 \) as above.
- For a trial value of \( n_2 \), compute \( P_{fe} \), \( P_{Cu1} \), \( P_{Cu2} \), and \( P_{tot} \) using above formulas.
- Try different values of \( n_2 \) until \( P_{tot} \) is minimized.
- Then compute wire sizes, gap length, etc.
Effect of transformer leakage inductance

Voltage clamp snubber

Leakage inductance $L_e$ is effectively in series with MOSFET $Q_1$.

When MOSFET switches off, it interrupts current flowing through $L_e$.

$L_e$ induces voltage spike according to:

$$v_L(t) = L_e \frac{di_L}{dt}$$

Transistor voltage waveform:

If the peak magnitude of the voltage spike exceeds the voltage rating of the MOSFET, then $Q_1$ will fail.
Protection of $Q_1$ using a voltage clamp snubber

- Snubber provides a path for $i_L$ to flow after $Q_1$ has turned off.
- Energy stored in $L_e = \frac{1}{2} L_e i_1^2 = \frac{1}{2} L_e I^2$ is transferred to $C_s$ and then is dissipated by $R_s$. Average power $= \frac{1}{2} L_e I^2 f_s$.
- Peak transistor voltage is clamped to $V_g + V_s > V_g + \frac{V_m}{n}$

An approach to select $R_s$ and $C_s$:
- Use large $C_s$ so that $V_s(t)$ has negligible ripple:
  \[ C_s \gg \frac{I_s}{R_s} \implies V_s(t) \approx V_s \]
- Voltage $V_s$ rises until power dissipated by $R_s$ is equal to average power transferred from $L_e$:
  \[ \frac{V_s^2}{R_s} = \frac{1}{2} L_e I^2 f_s \]
  \[ \implies \text{Choose } R_s \text{ such that } V_s \text{ is acceptably low} \]
- Note that $L_e$ depends on winding geometry and is not known until transformer is wound.
  - Measure $L_e$ on short circuit test, or guess its value.
Example - a first-pass selection of $R_s$ and $C_s$

Given $V_g = 150\text{V}$, $V = 15\text{V}$, $n = 0.2$

$f_s = 100\text{kHz}$, $L_m = 1\text{mH}$, $I = 1.5\text{A}$

HosFET peak voltage rating = 400V
It is desired to limit peak $v_T$ to 325V

Estimate $L_P$: in a good, carefully wound transformer, it may be possible to achieve $L_P = 3\%$ of $L_m = 30\mu\text{H}$

Energy stored in $L_P$ during $\Delta t + 2\Delta T_s$:

$W_s = \frac{1}{2} L_P I^2 = \left(\frac{1}{2}\right) (30\mu\text{H}) (1.5\text{A})^2 = 33.75\mu\text{J}$

Average power transferred from $L_P$ to snubber:

$P_s = W_s f_s = (33.75\mu\text{J}) (100\text{kHz}) = 3.375\text{W}$

To limit peak $v_T$ to 325V, we need

$V_s = \text{(peak } v_T) - V_g = 325 - 150 = 175\text{V}$

So choose $R_s = \frac{V_s^2}{P_s} = \left(\frac{175^2}{3.375\text{W}}\right) = 9074\Omega$

we might use a 10k$\Omega$, 5W resistor. Then

$C_s \gg \frac{T_f}{R_s} = \left(\frac{10\mu\text{s}}{10k\Omega}\right) = 1\text{nF}$

A good choice might be $C_s = 47\text{nF}$, 250V.

The above calculations are based on the estimate $L_P = 3\%$ of $L_m$, and should be considered first-pass estimates.