Adaptive Tuning of Digitally Controlled Switched Mode Power Supplies Based on Desired Phase Margin

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Abstract - This paper presents an online adaptive tuning technique for digitally controlled switched-mode power supplies (SMPS). The approach is based on continuous monitoring of the system crossover frequency and phase margin, followed by a multi-input multi-output (MIMO) control loop that continuously and concurrently tunes the compensator parameters to meet crossover frequency and phase margin targets. Small-signal models are derived and the MIMO control loop is designed to achieve stability and performance over a wide range of operating conditions. Using modest hardware resources, the proposed approach enables adaptive tuning during normal closed-loop SMPS operation. Experimental results demonstrating system functionality are presented for a synchronous buck SMPS.

I. INTRODUCTION

Switched-mode power supply (SMPS) feedback loops are typically designed conservatively so that closed-loop regulation and stability margins are maintained over expected ranges of operating conditions and tolerances in power stage parameters. Typical designs often lead to degraded closed-loop performance or loss of stability in the event of significant operating point changes associated with component degradation, input voltage variations, etc. These types of power stage parameter changes are mitigated by offline controller re-design to maintain desired dynamic performance constraints. With the increased feasibility of practical digital control for high-frequency switching power converters [1], new opportunities exist to incorporate intelligent control algorithms into the system to simplify the system design and improve dynamic responses and reliability over a wider range of possible operating points.

Recent work in the area of digital control of DC-DC power converters has shown that auto-tuning algorithms can be completely integrated into the digital controller with modest additional hardware requirements [2-10]. However, the approaches described in [2-10] in general require steady-state conditions during tuning, making them more suitable for one-time or periodic compensator auto-tuning. Direct application of [2-10] to continuous adaptation of compensator coefficients to account for changes in converter parameters or operating conditions is more difficult due to the steady-state requirement.

The goal of this paper is to present an approach to adaptive tuning of digital SMPS controller parameters during normal closed-loop operation of the converter. The proposed approach, which is related to a large body of work in adaptive control techniques [11-14], includes continuous monitoring of the system crossover frequency and phase margin [15], and a multi-input multi-output (MIMO) control loop that adaptively tunes the compensator parameters to meet crossover frequency and phase margin targets. In contrast to the solutions presented in [2-9], the tuning is not restricted to a one-time event, but rather initializes to a conservatively designed compensator and then continuously tunes the compensator coefficients to maintain desired system crossover frequency and phase margin. The adaptive tuning does not require undisturbed steady-state operation and causes a very small output voltage perturbation which allows the tuning to run continuously. Adaptive tuning can be used to improve closed-loop performance and reliability by maintaining stability margins over wide tolerances in power-stage parameters or variations in power stage operating conditions. Section II describes the proposed approach for adaptive tuning. Section III presents a numerical design procedure for the MIMO control loop. Experimental results are presented in Section IV using a synchronous buck converter power stage. Conclusions are presented in Section V.

II. ADAPTIVE TUNING SYSTEM

A system block diagram for the proposed tuning approach is shown in Fig. 1. The digital controller consists of a voltage A/D converter (ADC), a discrete-time PID compensator, and a digital pulse-width modulator (DPWM). There are two main components to the adaptive tuning system: a stability margin monitor [15] and a MIMO control loop. The stability margin monitor is a digital implementation of the analog loop gain measurement technique using signal injection, as first described by Middlebrook [16]. Details of the blocks required to implement the stability margin monitor are described in [15] and are only briefly discussed in this paper. The stability margin monitor is based on a variable frequency square-wave injection, \( V_s \), which is introduced between the output of the PID compensator and the DPWM input, similar to the technique described in [9]. The frequency of the perturbation, \( f_{inj} \), is adjusted via a feedback loop, until
and perturbation [15]. The injection signal magnitude, \( f_{inj} \), equals the system crossover frequency. Using the described system, both crossover frequency and phase margin can be continuously adjusted by the injection amplitude controller such that the gain \( K \) such that zero errors with respect to the target specifications are achieved. The matrix, \( S(z) \), represents the transfer functions from \( f_{c-error} \) and \( \varphi_{m-error} \) to \( K, Z_1 \) and \( Z_2 \). In the simplest case, the transfer functions are integrators,

\[
\begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2
\end{bmatrix} =
\begin{bmatrix}
A_1 \frac{z}{z-1} & A_2 \frac{z}{z-1} & \hat{f}_{c-error} \\
A_1 \frac{z}{z-1} & A_2 \frac{z}{z-1} & \hat{\varphi}_{m-error}
\end{bmatrix} = S(z) \begin{bmatrix}
\hat{f}_{c-error} \\
\hat{\varphi}_{m-error}
\end{bmatrix} .
\]

As shown in Fig. 1, the adaptive tuning controller is driven by the errors between the desired crossover frequency and phase margin and the values measured by the stability margin detector. The error signals, \( f_{c-error} \) and \( \varphi_{m-error} \), are inputs to a matrix of transfer functions used to determine the compensator zero locations, \( Z_1 \) and \( Z_2 \), and the gain \( K \) such that zero errors with respect to the target specifications are achieved. The matrix, \( S(z) \), represents the transfer functions from \( f_{c-error} \) and \( \varphi_{m-error} \) to \( K, Z_1 \) and \( Z_2 \). In the simplest case, the transfer functions are integrators,

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A_1 \frac{z}{z-1} & A_2 \frac{z}{z-1} & \hat{\varphi}_{m-error}
\end{bmatrix} = S(z) \begin{bmatrix}
\hat{f}_{c-error} \\
\hat{\varphi}_{m-error}
\end{bmatrix} .
\]

\[
\begin{bmatrix}
f_{inj} \\
\varphi
\end{bmatrix} =
\begin{bmatrix}
G_{f_{inj}-k} & G_{f_{inj}-z_1} & G_{f_{inj}-z_2} \\
G_{\varphi-k} & G_{\varphi-z_1} & G_{\varphi-z_2}
\end{bmatrix} \begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2
\end{bmatrix} = G(z) \begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2
\end{bmatrix} .
\]

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Together, (4) and (5) make up a system of loop gains associated with each loop in the MIMO system

\[ L(z) = G(z)S(z) = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix}. \]  

(6)

In (6), \( L_{11} \) and \( L_{22} \) represent the direct path loop gains while \( L_{12} \) and \( L_{21} \) represent coupling gains (i.e. from \( f_c \rightarrow \varphi_m \) and \( \varphi_m \rightarrow f_c \) respectively). Based on (6), each loop gain entry can be designed by choosing \( A_1-A_4 \), such that the closed-loop transfer matrix is stable and well-behaved. The closed-loop transfer matrix can be written in terms of the system of loop gains (6) as

\[
\begin{bmatrix} f_c \\ \varphi_m \end{bmatrix} = (I + L(z))^{-1} L(z) \begin{bmatrix} f_c_{\text{ref}} \\ \varphi_{m \text{ ref}} \end{bmatrix}. 
\]

(7)

Using (7), the stability of the MIMO control loop can be directly determined based on the location of the closed-loop poles. In particular, the closed-loop system described by (7) is exponentially stable if it is proper and has no poles outside the unit circle [17].

III. ADAPTIVE TUNING CONTROL LOOP DESIGN

The experimental test-bed, from which the design is performed, is a synchronous buck converter as shown in Fig. 1, with a digital feedback loop realized using a Xilinx Virtex-IV FPGA. The nominal power stage parameters in Fig. 1 are \( L = 4.0 \) \( \text{mH} \), \( C = 370 \) \( \mu \text{F} \), \( R = 2 \) \( \Omega \), \( V_i = 12 \) \( \text{V} \), \( V_{ou} = 5 \) \( \text{V} \) and \( f_c = 100 \) kHz. The ADC used to sample the output voltage is a TI-THS1030. The output voltage is sampled once per switching cycle with an effective output voltage LSB resolution of 20 mV, or 0.4 % of the DC output voltage.

In order to design (7) for desired performance and stability, the indices of (5) must first be determined. In this paper, the modeling is performed based on a design decision to make the stability margin monitor control loop much faster than the adaptive tuning control loop. This allows the dynamics associated with the stability margin monitor loop to be neglected by the adaptive tuning control loop. The waveforms illustrating the proposed modeling approach are given in Fig. 2, where, as an example, the effect of a perturbation in compensator gain \( K \) is considered. The perturbation, \( \hat{k}[n-1] \), occurs at time \((n-1)\) causing the stability margin monitor to update the new monitored crossover frequency \( f_c[n] \) very quickly with respect to the next sample of the MIMO control loop. The small-signal transfer function from \( \hat{k}[n-1] \) to \( f_c[n] \) is then just a one sample delay equal to \( T_{\text{sample}} \) and a gain scale factor, as indicated in Fig. 2. Also included in Fig. 2 is a corresponding simulation of the adaptive tuning system performed in Simulink. The simulation indicates that the bandwidth of the monitoring control loop can be designed to be much faster than the adaptive tuning control loop bandwidth, thus making the modeling approach valid.

In hardware, the sampling rates of both loops are set relative to the injection frequency (crossover frequency) with the stability monitoring loop having considerably faster sampling. By doing so, as the injection frequency changes, the sample rates of each loop will scale in proportion to each other thus maintaining the same relative speeds of the control loops. In the experimental system, the sampling rate of the stability margin monitor control loop is set to 16 times slower than the injection frequency while the adaptive tuning loop sampling rate is set to 64 times slower than the injection frequency.

Based on the power stage defined above, using a small-signal model [18], a nominal PID compensator can be designed for the output voltage feedback loop to yield relatively slow but guaranteed stable performance. It is assumed that sufficient information about the nominal power stage (i.e. at system startup) is known such that a conservative compensator design can be performed. Given the experimental system, the following compensator was used for system initialization

\[ G_c(z) = 1.0 \frac{(z - 0.90)(z - 0.80)}{(z - 1)}. \]  

(8)

which yields a system crossover frequency \( f_c = 6.2 \) kHz and phase margin \( \varphi_m = 65^\circ \). Now, using the defined power stage and the compensator given in (8) as the adaptive tuning DC operating point, the small-signal gains given in \( G(z) \) have been numerically computed based on the previously described modeling approach

\[
\begin{bmatrix} f_c \\ \varphi \end{bmatrix} = \begin{bmatrix} -4577 & -1138 \\ 470 & 1918 \\ 2102 & 2239 \end{bmatrix} \begin{bmatrix} \hat{k} \\ \hat{\varphi} \end{bmatrix}. 
\]

(9)

With numerical values for the indices of \( G(z) \) as given in (9), the closed-loop response can be shaped using (4) to
achieve desired performance. As an example, consider
the following choice

\[ A_2 = A_1 = A_3 = 0. \]  \(10\)

The constraints given in (10) are not required; however, (10) simplifies the design of the adaptive tuning control system. The primary limitation introduced by (10) is that \( L_{11} \) and \( L_{21} \) in (6) can only be shaped by the choice of \( A_1 \).

Beyond the constraints given in (10), the adaptive tuning gains can be designed to achieve desired performance and stability as discussed previously. In the experimental system, the adaptive tuning control loop has been designed to minimize phase margin error faster than the crossover frequency error. This amounts to choosing \( A_1 \), \( A_4 \) and \( A_6 \) such that the closed-loop bandwidth of the direct phase margin loop is greater than the direct crossover frequency path bandwidth. To realize this, the gains in the experimental system were chosen as follows

\[
\begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2
\end{bmatrix} =
\begin{bmatrix}
\frac{z - 3.05 \times 10^{-5}}{z - 1} & 0 & 0 \\
0 & \frac{z - 1.14 \times 10^{-4}}{z - 1} & \hat{f}_c \text{ error} \\
0 & \frac{z - 1}{z - 1.38 \times 10^{-4}} & \hat{\phi}_m \text{ error}
\end{bmatrix},
\]  \(11\)

which leads to a system loop gain matrix of:

\[
L(z) = \begin{bmatrix}
0.14 & 0.05 \\
-0.0143 & 0.4 \\
-0.14 & 0.05
\end{bmatrix}.
\]  \(12\)

The impact of this design can be discussed based on the closed-loop frequency responses, computed from (7) and (12), and given in Fig. 3. Fig. 3(a) is the closed-loop frequency response from \( f_c \) to \( f_{c_{\text{ref}}} \) indicating that crossover frequency reference changes are tracked well up to about 10 Hz, which is the approximate bandwidth of that tuning loop. Similar results are presented in Fig. 3(d) showing that the effect of \( \phi_{m_{\text{ref}}} \) changes on \( \phi_m \) are tracked up to about 40 Hz. Conversely, Fig. 3(b) is the response of \( \phi_m \) to changes in \( f_{c_{\text{ref}}} \) showing that any changes in \( f_{c_{\text{ref}}} \) do not significantly affect \( \phi_m \) due to the action of the feedback loop. Similarly, Fig. 3(c) indicates that \( f_c \) is not significantly affected by \( \phi_{m_{\text{ref}}} \) changes. Note that the closed-loop bandwidth of the \( \phi_m \) to \( \phi_{m_{\text{ref}}} \) loop is the largest thus ensuring fastest convergence of the phase margin loop.

Figure 4 shows the step response predicted by the model (red) and the simulated (performed in Simulink) response (blue). First note that from Fig. 4, the predicted step responses, based on the derived models, of each loop match the simulated result, indicating the modeling approach presented previously is in fact valid. In Fig. 4(a) and Fig. 4(d), note that a step in phase margin

![Figure 3](image-url)

**Figure 3.** Closed-loop frequency response of MIMO control system from: (a) \( f_c \) to \( f_{c_{\text{ref}}} \), (b) \( \phi_m \) to \( f_{c_{\text{ref}}} \), (c) \( f_c \) to \( \phi_{m_{\text{ref}}} \), (d) \( \phi_m \) to \( \phi_{m_{\text{ref}}} \).

Responses (a) and (d) show that \( f_c \) and \( \phi_m \) track well the reference values up to a given frequency, while (b) and (c) show rejection of cross-coupling, as desired.
assumes the other parameters are at nominal values. Table I that any one of the power stage variations instability in the adaptive tuning feedback loops. Note in components can tolerate large changes without inducing stable. As indicated, all three major power stage adaptive tuning loops, with gains given by (11), remain allowable power stage variations under which the poles of the MIMO adaptive tuning control loops remain stable (i.e. the closed-loop (13), which lie inside the unit circle.

Finally, because the adaptive tuning system is being designed to account for potentially large power stage variations, it is of interest to investigate the range of power stage component changes under which the adaptive tuning loop remains stable (i.e. the closed-loop poles of the MIMO adaptive tuning control loops remain inside the unit circle). Table I shows the range of allowable power stage variations under which the adaptive tuning loops, with gains given by (11), remain stable. As indicated, all three major power stage components can tolerate large changes without inducing instability in the adaptive tuning feedback loops. Note in Table I that any one of the power stage variations assumes the other parameters are at nominal values.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>570 μF</td>
<td>1.6 mF</td>
<td>15 μF</td>
</tr>
<tr>
<td>L</td>
<td>4.0 μH</td>
<td>17 μH</td>
<td>0.35 μH</td>
</tr>
<tr>
<td>Vgs</td>
<td>12 V</td>
<td>17 V</td>
<td>3 V</td>
</tr>
</tbody>
</table>

IV. EXPERIMENTAL RESULTS

Experimental verification was performed on the same hardware as described in Section III. The adaptive tuning process begins by initializing the system to the nominal compensator given by (8). For this experiment, the target crossover frequency is set at $f_{c_{ref}} = 14.6$ kHz and the target phase margin is $\phi_{m_{ref}} = 40^\circ$. Figure 5 shows how the compensator parameters adjust to meet target stability specifications from start-up, with the compensator given by (8), to steady state when the stability margin references are met. As shown in Fig. 5, after a short time, the compensator parameters converge to

$$G_c(z) = \frac{3.63(z-0.9492)(z-0.8203)}{z(z-1)^2}.$$ (14)

Based on the discrete-time model of [18], the analytical crossover frequency and phase margin are $f_{c_{analytical}} = 14.5$ kHz and $\phi_{m_{analytical}} = 39$, which both closely match the target values, and the values measured by the stability margin monitor. Further examples illustrating the monitor performance can be found in [15].

Figure 6 is a comparison of load transient performance between the conservatively designed control loop corresponding to the compensator given by (8) and the above described adaptive loop with target crossover frequency $f_{c_{ref}} = 14.6$ kHz, and desired phase margin $\phi_{m_{ref}} = 40^\circ$. The conservatively designed control loop exhibits noticeably worse load transient performance after a change in input voltage or output filter capacitance. With the adaptive tuning system running, the PID compensator is automatically adjusted to maintain reference phase margin and crossover frequency in the presence these system changes. As a consequence, the load transient performance is not degraded when the adaptive tuning is running. In Figs. 6(d), 6(e) and 6(f), the amplitude of the oscillation due to the signal

![Figure 4](image.png)

Figure 4. Predicted and simulated normalized step responses for MIMO control loop from: (a) $f_c \rightarrow f_{c_{ref}}$; (b) $\phi_m \rightarrow \phi_{m_{ref}}$; (c) $f_c \rightarrow \phi_{m_{ref}}$; (d) $\phi_m \rightarrow \phi_{m_{ref}}$.

reference is tracked faster than a step in crossover frequency, as expected based on the closed-loop frequency responses given in Fig. 3. Conversely, Fig. 4(b) and 4(c) indicate that the cross-coupling gains do not strongly respond to step reference changes.

As indicated in Fig. 4, all closed-loop responses are stable and well-behaved. This is further validated by inspection of the closed-loop poles of the system based on the design given in (11). Specifically, for the design given by (11), each of the indices of the closed-loop transfer matrix share the same closed loop poles, given by $z_1 = 0.8561$ and $z_2 = 0.6039$.

![Figure 5](image.png)

Figure 5: Experimentally observed dynamic performance of the MIMO adaptive tuning control loop. (a) Monitored phase margin in degrees; (b) PID compensator z-domain zero locations; (c) Monitored crossover frequency in kHz; (d) PID compensator gain

![Figure 6](image.png)

Figure 6: Figure 6 is a comparison of load transient performance between the conservatively designed control loop corresponding to the compensator given by (8) and the above described adaptive loop with target crossover frequency $f_{c_{ref}} = 14.6$ kHz, and desired phase margin $\phi_{m_{ref}} = 40^\circ$. The conservatively designed control loop exhibits noticeably worse load transient performance after a change in input voltage or output filter capacitance. With the adaptive tuning system running, the PID compensator is automatically adjusted to maintain reference phase margin and crossover frequency in the presence these system changes. As a consequence, the load transient performance is not degraded when the adaptive tuning is running. In Figs. 6(d), 6(e) and 6(f), the amplitude of the oscillation due to the signal
Figure 6. AC coupled output voltage (top) and inductor current (bottom) in the presence of load transients. (a)-(c) are load transient results without adaptive tuning, (d)-(f) are load transient results with adaptive tuning.

<table>
<thead>
<tr>
<th>Without Adaptive Tuning</th>
<th>With Adaptive Tuning</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vg = 12V C = 370 μF</td>
</tr>
<tr>
<td>Measured Crossover</td>
<td>6.2 kHz</td>
</tr>
<tr>
<td>Frequency</td>
<td></td>
</tr>
<tr>
<td>Measured Phase Margin</td>
<td>65°</td>
</tr>
<tr>
<td>% Overshoot</td>
<td>4%</td>
</tr>
<tr>
<td>Settle Time</td>
<td>80 μs</td>
</tr>
<tr>
<td>Compensator G(z)</td>
<td>( \frac{1}{z(0.90^2 - 0.80)} )</td>
</tr>
</tbody>
</table>
injection $V_i$ is about ± 1 LSB of the voltage sensing ADC, which equals ± 0.4% of the DC output voltage. A summary of the load transient performance and the adaptively tuned compensators is given in Table II. As indicated, with the adaptive tuning, load transient performance is not compromised in the presence of system variations. As a final note, Table III lists the required logic resources to implement the above described adaptive tuning system and phase margin monitor. Table III indicates that for a reasonable number of gates and no memory requirements, the adaptive tuning controller can be added to a digital controller to simplify system design and improve reliability and performance.

<table>
<thead>
<tr>
<th>Function</th>
<th>Logic Gates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Injection/Clock Generator</td>
<td>1262</td>
</tr>
<tr>
<td>Stability Margin Monitor</td>
<td>4594</td>
</tr>
<tr>
<td>Amplitude Controller</td>
<td>1448</td>
</tr>
<tr>
<td>Adaptive Tuning Control Loop</td>
<td>4262</td>
</tr>
<tr>
<td>PID Compensator</td>
<td>1704</td>
</tr>
<tr>
<td>Total</td>
<td>13270</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

This paper presents a practical method for online adaptive tuning of digital controllers for switched mode power supplies (SMPS). The compensator tuning relies on continuous monitoring of phase margin and crossover frequency, which are outputs of a stability margin monitor [15]. The monitored phase margin and crossover frequency are inputs to a multi-input multi-output (MIMO) control loop which minimizes the error between the desired crossover frequency and phase margin and the measured values. Simple small-signal models are derived and used to design the adaptive tuning control loop to achieve stability over a wide range of power stage parameters and operating points. Experimental results presented for a synchronous buck SMPS demonstrate improved load transient performance, indicating that more aggressive design and more robust system performance can be achieved with the adaptive tuning system as compared to conventional controller designs. Hardware requirements for the entire adaptive tuning system are relatively modest making it a practical solution for high performance digitally controlled DC-DC power converters.

REFERENCES