Adaptive Tuning of Switched-Mode Power Supplies Operating in Discontinuous and Continuous Conduction Modes

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Abstract—This paper presents an approach to adaptive tuning of voltage-mode digital controllers for switched-mode power supplies in the presence of large signal changes from discontinuous conduction mode (DCM) to continuous conduction mode (CCM) and vice versa. The approach is capable of maintaining a high-performance control loop without the stability issues related to DCM-to-CCM mode transitions. The adaptive tuner, modeled as a multiple-input–multiple-output (MIMO) controller, is designed to continuously adjust the parameters of a PID compensator such that crossover frequency and phase margin measured by the digital controller match desired values. A simplified design procedure for the adaptive tuning system is proposed that reduces the small-signal MIMO design into two independent single-input, single-output control loops. Simulation results are given showing that despite wide uncertainty in the power stage, the adaptive tuning system still converges to the desired stability margins. Experimental results are given using an 11- to 5-V, 45-W, DCM/CCM buck converter as a test bed.

Index Terms—Adaptive control, dc–dc power conversion, digital control.

I. INTRODUCTION

DIGITAL controllers have been gaining popularity in switched-mode power supply (SMPS) systems due to the increased demand for intelligent control algorithms capable of improving performance while maintaining system robustness. These algorithms become especially important when widely varying converter dynamics are expected. For example, in many SMPS applications, operation in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM) is possible depending on the load current. In conventional voltage-mode controller designs, it is well known that variations in converter operating mode can cause large changes in the plant dynamics. Analog voltage-mode controllers often cope with this problem by operating at a relatively low control bandwidth to ensure stability at the worst-case operating point. Whenever this conservative design appears unacceptable for the specific application, a common choice is analog current-mode control, which is less critical with respect to converter operating point variations at the cost of added complexity.

An alternative offered by digital controllers is investigated in this paper, which maintains the voltage-mode controller without sacrificing system performance by employing a digital controller equipped with adaptive tuning capabilities. Autotuning or adaptive tuning algorithms offer the potential to improve dynamic performance in the presence of variations by automatically adjusting control loop parameters. Further, it is relatively easy to integrate these algorithms into a standard digital controller, while maintaining simplicity and low cost [1].

Beginning with a typical implementation of a standard digital voltage-mode controller, consisting of an A/D converter (ADC), a digital compensator, $G_c(z)$, and a digital pulsewidth modulator (DPWM), a number of autotuning algorithms have been proposed as add-ons to the core controller [2]–[5]. The plant control-to-output frequency response is identified in [2] and [3], and used to tune the parameters of a PID compensator. However, the plant identification itself requires steady-state operation, and the proposed tuning of the compensator parameters is performed in a series of steps. For these reasons, this solution is best suited for one-time parameter tuning, for example, upon startup. Similarly, [4] and [5] propose autotuning methods that induce limit-cycle oscillations into the system for the purpose of tuning compensator parameters. However, similar to [2] and [3], the tuning runs in a series of steps, thus making continuous parameter tuning more difficult to apply. Without the ability to tune the compensator parameters continuously, these algorithms are unable to account for some of the variations typical to normal SMPS operation. Continuous parameter tuning (i.e., adaptive tuning) has been a major focus of research in controls literature for many years [6]. Recently, some of these approaches have been applied in various forms to adaptive tuning of SMPS systems [7]–[9]. This paper aims to extend the work presented in [7]–[9] by introducing an adaptive tuner for voltage-mode digital controllers capable of operating under major changes in the converter dynamics such as DCM-to-CCM mode transitions. The proposed implementation of the adaptive tuner applied to a digitally controlled buck SMPS is given in Fig. 1.

This paper is organized as follows. A brief overview of the approach used to tune the compensator parameters together with a simplified small-signal design procedure for the adaptive tuning system are described in Section II. Next, Section III discusses large-signal design considerations in the context of transients from DCM to CCM and vice versa. A modification to the...
II. ADAPTIVE CONTROLLER DESIGN

The implementation of the core adaptive tuning system, first proposed in [8] and [9], is shown in Fig. 2. A variable frequency, 50% duty cycle digital square-wave perturbation, \( V_z \), is injected into the control loop between the compensator output and the DPWM input. After some simple digital filtering, it can be shown that the loop gain \( T \) can be found directly by

\[
T = \frac{-V_y}{V_x}. \tag{1}
\]

Given (1), the digital stability margin monitor adjusts the frequency of \( V_z \) via a feedback loop until

\[
\|V_y\| = \|V_x\| \tag{2}
\]

at which point the injection frequency is equal to the loop crossover frequency \( f_c \). Similarly, the loop gain phase margin can be measured directly as

\[
\phi_m = \angle V_y - \angle V_z. \tag{3}
\]

Using (2) and (3), the stability margin monitor can be used to measure crossover frequency and phase margin online in a digitally controlled converter without requiring open-loop or steady-state operation. During the system operation, a small output voltage perturbation is imparted by \( V_z \). However, it has been shown that the amplitude of \( V_z \) can be automatically adjusted to minimize the perturbation amplitude to \( \pm 1 \) LSB of the output voltage ADC [12]. Accuracy of the stability margin monitor has been demonstrated over a range of converter topologies and operating modes in [12].

Using the outputs of the stability margin monitor \( f_c \) and \( \phi_m \), an adaptive tuning system compares the measured stability margins to reference values \( f_{c,ref} \) and \( \phi_{m,ref} \), which define the desired crossover frequency and phase margin. The errors between desired and measured stability margins are processed via the adaptive controller such that the parameters \( K, Z_1, \) and \( Z_2 \) of the PID compensator, given by

\[
G_c(z) = K \frac{(z - Z_1)(z - Z_2)}{z(z - 1)} \tag{4}
\]

can be adjusted. The adaptive tuning controller can be modeled as a multiple-input–multiple-output (MIMO) control loop from which stability analysis can be performed by first splitting the MIMO system into two transfer matrices. The first transfer matrix represents the dynamics of the MIMO plant, defined here as

\[
\begin{bmatrix}
\hat{f}_c \\
\hat{\phi}_m \\
\end{bmatrix} =
\begin{bmatrix}
G_{f_c-K} & G_{f_c-Z_1} & G_{f_c-Z_2} \\
G_{\phi_m-K} & G_{\phi_m-Z_1} & G_{\phi_m-Z_2} \\
\end{bmatrix}
\begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2 \\
\end{bmatrix}
\]

\[
= G(z_t)
\begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2 \\
\end{bmatrix}
\]

(5)

with

\[
z_t = e^{sT_{sample}} \tag{6}
\]

where \( T_{sample} \) is the sample period of the adaptive tuning system.

The matrix elements in (5) can be modeled as a simple gain and delay, as described in [9]. The second transfer matrix \( S(z_t) \) represents the compensator for the MIMO adaptive control.
loop and is given by
\[
\begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2
\end{bmatrix} = \begin{bmatrix}
A_1 \frac{z_1}{z_1 - 1} & A_2 \frac{z_1}{z_1 - 1} & \hat{f}_{c,\text{error}} \\
A_3 \frac{z_1}{z_1 - 1} & A_4 \frac{z_1}{z_1 - 1} & \hat{\phi}_m \hat{f}_{c,\text{error}} \\
A_5 \frac{z_1}{z_1 - 1} & A_6 \frac{z_1}{z_1 - 1} & \hat{\phi}_m \hat{f}_{c,\text{error}}
\end{bmatrix} \begin{bmatrix}
S(z_t) \\
\hat{f}_{c,\text{error}} \\
\hat{\phi}_m \hat{f}_{c,\text{error}}
\end{bmatrix} = \begin{bmatrix}
L_{11} & L_{12} & \hat{f}_{c,\text{error}} \\
L_{21} & L_{22} & \hat{\phi}_m \hat{f}_{c,\text{error}}
\end{bmatrix} \begin{bmatrix}
L(z_t) \\
\hat{f}_{c,\text{error}} \\
\hat{\phi}_m \hat{f}_{c,\text{error}}
\end{bmatrix},
\tag{7}
\]

where \(S(z_t)\) can be designed such that the system is stable and well behaved. The stability was investigated in [9] by computing the MIMO loop gain as
\[
L(z_t) = G(z_t)S(z_t) = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \tag{8}
\]

and then determining the locations of the closed-loop poles of the MIMO system from the closed-loop transfer matrix as
\[
\begin{bmatrix}
\hat{f}_c \\
\hat{\phi}_m
\end{bmatrix} = (I + L(z_t))^{-1} L(z_t) \begin{bmatrix}
\hat{f}_{c,\text{error}} \\
\hat{\phi}_m \hat{f}_{c,\text{error}}
\end{bmatrix}. \tag{9}
\]

A difficulty with this approach is that the expressions for the closed-loop poles are often very complicated, yielding little insight into how the indexes of (7) should be chosen.

In this paper, a different technique is proposed in which the MIMO design is based directly on (8) rather than (9), thus significantly simplifying the design procedure. The approach begins by defining the desired MIMO loop gain \(L(z_t)\) as
\[
\hat{L}(z_t) = \begin{bmatrix} \hat{L}_{11} & \hat{L}_{12} \\ \hat{L}_{21} & \hat{L}_{22} \end{bmatrix} = \begin{bmatrix} K_{11} (z_t - 1)^{-1} & 0 \\ 0 & K_{22} (z_t - 1)^{-1} \end{bmatrix}. \tag{10}
\]

Using (10), the proposed design approach consists of calculating \(S(z_t)\) such that the actual MIMO loop gain matches the desired loop gain \((L(z_t) = \hat{L}(z_t))\) at a nominal converter operating point.

Intuitively, constraining \(\hat{L}_{12} = \hat{L}_{21} = 0\) decouples the MIMO system into two independent single-input–single-output (SISO) control loops. When \(L(z_t) = \hat{L}(z_t)\), changes in \(f_{c,\text{error}}\) have no effect on the loop phase margin \(\hat{\phi}_m\). Similarly, changes in \(\hat{\phi}_m \hat{f}_{c,\text{error}}\) have no effect on the crossover frequency \(f_c\). This simplification allows the stability of the entire adaptive controller to be determined by the two, independent direct path loop gains. The target loop gains \(L_{11}\) and \(L_{22}\) have both been set to simple integrators with gains based on the desired performance of the two decoupled SISO loops.

Based on (10), the control loop design has been simplified to four constraints [shape of each index of \(\hat{L}(z_t)\)] and six unknowns \((A_1, A_2, A_3)\). A further simplifying constraint is imposed on the adaptive controller to reduce the number of unknowns to four
\[
A_2 = A_3 = 0. \tag{11}
\]

With (10) and (11) satisfied, the control loop gain is reduced to a system of four linear equations with four unknowns \((A_1, A_4, A_5, A_6)\), which can be solved to yield the desired adaptive tuning control law.
(\(K_{CCM}, Z_{1,CCM}, \) and \(Z_{2,CCM}\)), each employed and tuned during DCM and CCM operation, respectively. Upon a mode transition, the proper set of parameters, tuned for the specific operating mode, is loaded into the output voltage loop compensator.

In what follows, it is assumed that the converter operating mode is detected and indicated by a logic level signal \(Mode_L\) (e.g., \(Mode_L = 1\) for DCM operation and \(Mode_L = 0\) for CCM operation). The details of generating \(Mode_L\) are given in Section III-B.

As shown in Fig. 3, in the modified adaptive tuner the single \(S(z)\) transfer matrix from (7) is replaced with two effective transfer matrices, one for operation in CCM

\[
S_{CCM}(z) = \begin{bmatrix} S_{1,CCM} & S_{2,CCM} \\ S_{3,CCM} & S_{4,CCM} \\ S_{5,CCM} & S_{6,CCM} \end{bmatrix}
\]  

(12)

and another for operation in DCM

\[
S_{DCM}(z) = \begin{bmatrix} S_{1,DCM} & S_{2,DCM} \\ S_{3,DCM} & S_{4,DCM} \\ S_{5,DCM} & S_{6,DCM} \end{bmatrix}
\]  

(13)

Upon system startup, each set of transfer matrices is initialized to output the same PID compensator parameter values in both modes, \(K_{CCM} = K_{DCM}, Z_{1,CCM} = Z_{1,DCM},\) and \(Z_{2,CCM} = Z_{2,DCM}\). The initial compensator values are designed to realize a conservative controller that guarantees stable operation of the output voltage control loop. Note that according to the design procedure outlined in Section II, \(A_2 = A_3 = 0\) in the implementation of Fig. 3.

When the power stage is in DCM (\(Mode_L = 1\)), the tuning system operates by updating \(K_{DCM}, Z_{1,DCM},\) and \(Z_{2,DCM}\) based on \(S_{DCM}(z)\) in order to zero the error between desired and measured stability margins. Simultaneously, the inputs to \(S_{CCM}(z)\) are held at zero such that the CCM PID compensator parameters remain unchanged. At the adaptive tuner output, \(Mode_L\) is used to load the DCM compensator parameters into the voltage loop compensator \(G_c(z)\). Conversely, when the converter is operating in CCM (\(Mode_L = 0\)), CCM compensator parameters are tuned and loaded into \(G_c(z)\), while the inputs to \(S_{DCM}(z)\) are held at zero so that the most recent DCM compensator parameters are stored.

Upon mode transitions, the PID compensator parameters abruptly switch so that the compensator \(G_c(z)\) corresponds to the correct mode of operation. Immediately following the mode switch, the adaptive tuning continues as usual, updating the compensator parameters based on the measured errors in the stability margins. With the proposed modification to the adaptive tuner, a high-bandwidth output voltage control loop is available in both operating modes without the stability issues associated with mode transitions.

B. DCM/CCM Detection Circuit

To implement the modified adaptive controller described in Section III-A, a sensor is proposed that is capable of determining the converter mode of operation (CCM or DCM) and generating the signal \(Mode_L\). The sensor, applied to a buck SMPS, is shown in Fig. 4(a) along with idealized waveforms describing its operation given in Fig. 4(b). The switched-mode voltage \(v_{sw}\) (from Fig. 1) is compared to zero (ground). When \(v_{sw}\) is above zero, the comparator output is high, while when \(v_{sw}\) is below zero (the power stage diode conducts with a forward voltage drop \(V_d\)), the comparator output is low. A Zener diode clamps the comparator noninverting input below the positive supply rail. Note that in Fig. 4(a), the comparator negative rail is tied to ground, thus requiring a comparator with input common-mode range that extends below ground.

The logic-level comparator output signal \(Mode\) is sampled immediately before the DPWM rising edge (which is internally available in the digital controller). If \(Mode\) is high at this sample instant, the converter is operating in DCM. Conversely, if sampled \(Mode\) is low, the converter is operating in CCM. Finally, debouncer logic provides a form of hysteresis in the mode detection, which is necessary in the case of a fast load transient causing multiple transitions to/from CCM or DCM before settling to a new steady state. The debouncer logic is configured such that the output (\(Mode_{DB}\)) latches immediately during a transition from DCM to CCM and does not allow another \(Mode_{DB}\) transition until a certain number of consecutive CCM samples (six

Fig. 4. (a) DCM/CCM detection circuit. (b) Idealized DCM/CCM detection waveforms under a transient from DCM to CCM.
in the experimental prototype) are detected. Conversely, a load transient from CCM to DCM is configured such that Mode_DB updates to Mode_L after six consecutive samples of DCM operation to ensure the converter has truly transitioned to DCM. The sensing of mode transitions. However, the PID compensator $G_c(z)$ continues to operate on the voltage error with a very small loop delay (less than one switching period at all times).

IV. DESIGN EXAMPLE AND PERFORMANCE ANALYSIS

In this section, a design example for the adaptive controller is shown based on the approach described in Section II. Using this design, which is based on a predefined nominal converter operating point, the effect of uncertainty and/or variations in the power stage is then investigated through a set of Simulink simulations. For reference, the simulation test bed is the buck converter power stage, as shown in Fig. 1. The nominal parameters of the power stage are $V_g = 11$ V, $V = 5$ V, $C = 110$ µF, $L = 0.6$ µH, and $f_s = 390$ kHz. The load resistance $R_{load}$ can have three distinct values with $R_{load} = 0.55$ Ω resulting in CCM, while $R_{load} = 5$ Ω or $R_{load} = 10$ Ω result in two different DCM operating points.

The adaptive tuning controller was designed using the procedure described in Section II, based on the power stage operating in CCM at $R_{load} = 0.55$ Ω. Upon startup, the adaptive tuning controller initializes to a conservative compensator

$$G_c(z) = 1.35(z - 0.85)(z - 0.7) \over (z - 1)$$

which results in stable, well-behaved closed-loop operation for all expected loads. In particular, the $G_c(z)$ compensator of (14) results in a crossover frequency of $38$ kHz ($\sim 1/10 f_s$) and $\phi_m = 40^\circ$ at the nominal CCM operating point ($R_{load} = 0.55$ Ω). With a change in $R_{load}$ to $5$ Ω, the power stage will nominally operate in DCM and the crossover frequency decreases to $5.1$ kHz with $\phi_m = 44.5^\circ$. For $R_{load} = 10$ Ω, the crossover frequency is $f_c = 4.25$ kHz and the phase margin is $\phi_m = 35^\circ$.

Based on the CCM operating point and by use of the modeling technique described in [9], the $G(z_l)$ transfer function from (5) has been derived as

$$G(z_l) = \begin{bmatrix} -1269 & -121.6 & 869 \\ z_l & z_l & z_l \\ -55 & 447.9 & 458.5 \\ z_l & z_l & z_l \end{bmatrix}.$$  

(15)

Following the design procedure outlined in Section II, the target MIMO loop gain has been defined as

$$\tilde{L}(z_l) = \begin{bmatrix} 0.05(z_l - 1)^{-1} & 0 \\ 0 & 0.25(z_l - 1)^{-1} \end{bmatrix}.$$  

(16)

Based on (16), the nominal adaptive tuning control law can be found assuming CCM operation as

$$S(z_l) = \begin{bmatrix} -4.3 \times 10^{-5} \frac{z_l}{z_l - 1} & 0 \\ 0 & 4.9 \times 10^{-4} \frac{z_l}{z_l - 1} \end{bmatrix} \quad (17)$$

Note that the tuner was designed so that $S(z_l) = S_{CCM}(z_l) = S_{DCM}(z_l)$.

Fig. 5 shows the predicted closed-loop step responses, based on the models derived previously, of the adaptive controller at the three different power stage operating points. Fig. 5(a) and (d) show the direct term responses from $f_{c,ref}$ to $f_c$ and $\phi_{m,ref}$ to $\phi_m$, and indicate good tracking of the reference variables. Further, the results verify that the phase margin tracking-loop bandwidth is higher than that of the crossover frequency tracking loop, which ensures that phase margin is given the highest priority in the adaptive controller. Finally, Fig. 5(b) and (c) shows that the cross-coupling terms in the MIMO system do not respond to step reference changes at the nominal CCM power stage operating point, as expected from the target loop gain in (16).

In order to understand the effect of power stage variations on the MIMO control loop behavior, operation away from the nominal CCM operating point has been investigated. Fig. 5 also shows the effect of using $S(z_l)$ designed for CCM while operating in DCM [i.e., $S(z_l) = S_{CCM}(z_l) = S_{DCM}(z_l)$]. With changes in $R_{load}$, (16) is no longer the actual MIMO plant transfer function, and hence, $L_{12} \neq L_{21} \neq 0$. This results in small coupling of the adaptive control loops, as shown in Fig. 5(b) and (c). Nevertheless, in spite of these nonideal interactions, good tracking of the reference variables is still achieved with the nominal adaptive control loop design.

The results summarized by the step responses in Fig. 5 are valid at system startup, corresponding to the $G_c(z)$ given by (14). However, the aforementioned results do not predict the adaptive system behavior beyond startup (after $K$, $Z_1$, and $Z_2$ begin changing) or with wide uncertainty in power stage parameters $L$, $C$, $V_g$, or $R_{load}$. To investigate the trajectories of the adaptive tuning system beyond startup while simultaneously taking into account wide uncertainty in the power stage, a corner analysis has been performed in simulation. The system simulation, implemented using MATLAB/Simulink, consists of an ideal stability margin monitor along with the full adaptive tuning system described previously. Wide uncertainties in $V_g$, $L$, $C$, and $R_{load}$ are investigated by running a set of simulations assuming worst-case variations in the power stage parameters. In doing so, a large-signal analysis of the robustness of the adaptive tuning system to wide uncertainty in the power stage can be obtained.

Fig. 6 presents 15 worst-case simulated corners, showing crossover frequency versus phase margin with $f_{c,ref} = 55$ kHz and $\phi_{m,ref} = 40^\circ$. In Fig. 6, operation in DCM is denoted by the solid lines, while operation in CCM is denoted by the dashed lines. For each simulation run, the initial conditions for the
adaptive tuning system are represented by the dots shown in Fig. 6. The range of worst-case variations in power stage parameters is summarized in Table I. As indicated in Fig. 6, even when operating at the worst-case corners in power stage parameters, both crossover frequency and phase margin converge to the reference values (i.e., zero error in desired versus measured stability margins) based on the nominal design given in (17). Also shown in Fig. 6 is the adaptive tuner response under the nominal power stage operating point, indicated by the gray line.

![Fig. 5](image1)

![Fig. 6](image2)

**Fig. 5.** Predicted closed-loop step responses of the adaptive tuning control loop with $R_{\text{load}} = 0.55 \, \Omega$, $R_{\text{load}} = 5 \, \Omega$, and $R_{\text{load}} = 10 \, \Omega$ using a fixed $S_{\text{CM}}(z)$. (a) $f_c/f_{\text{ref}}$. (b) $\phi_m/f_{\text{ref}}$. (c) $f_c/\phi_{\text{ref}}$. (d) $\phi_m/\phi_{\text{ref}}$.

**Fig. 6.** Simulated $f_c$ versus $\phi_m$ over worst-case corners in power stage parameters $C$, $L$, $V_g$, and $R_{\text{load}}$. Solid lines indicate the power stage is operating in DCM, while dashed lines indicated CCM operation. Gray line indicates tuner response with nominal power stage parameters.

<table>
<thead>
<tr>
<th>Power Stage Parameter</th>
<th>Nominal Value</th>
<th>Maximum Value</th>
<th>Minimum Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C$ +/- 50%</td>
<td>1.0 $\mu$F</td>
<td>1.65 $\mu$F</td>
<td>0.55 $\mu$F</td>
</tr>
<tr>
<td>$L$ +/- 30%</td>
<td>0.6 $\mu$H</td>
<td>0.78 $\mu$H</td>
<td>0.42 $\mu$H</td>
</tr>
<tr>
<td>$V_g$ +/- 30%</td>
<td>11 $V$</td>
<td>14.3 $V$</td>
<td>7.7 $V$</td>
</tr>
<tr>
<td>$R_{\text{load}}$</td>
<td>0.55 $\Omega$</td>
<td>10 $\Omega$</td>
<td>0.1 $\Omega$</td>
</tr>
</tbody>
</table>

**V. EXPERIMENTAL RESULTS**

To verify the adaptive tuning system experimentally, the buck converter power stage and associated adaptive tuning system design described in Section IV is again used. A TI-THS1030 ADC samples the output voltage once per switching period immediately before the rising edge of the trailing-edge DPWM output signal. The DPWM is an 11-bit hybrid DPWM clocked at 25 MHz. The digital controller, including the PID compensator, DPWM, stability margin monitor, and adaptive tuner were written in Verilog HDL and implemented on a Virtex-IV field-programmable gate array (FPGA) development platform.

The DCM/CCM sensor, shown in Fig. 4(a), uses an LMV7219 comparator with an input common mode extending 200 mV below the ground, as is necessary for the proposed sensor implementation. A 1N523B Zener diode clamps the comparator input voltage at 2.7 V. The series resistor [$R_c$ in Fig. 4(a)] is 390 $\Omega$.

The initial PID compensator $G_c(z)$ is shown in (14). As mentioned previously, based on a discrete-time modeling technique [14], the compensator of (14) results in a crossover
Fig. 7. Comparison of various load transient responses with conventional, fixed compensator versus the adaptive tuning system using $f_{c,ref} = 55$ kHz and $\varphi_{m,ref} = 40^\circ$. (a) $R_{load} = 10 \Omega \rightarrow R_{load} = 0.55 \Omega$ with a fixed compensator. (b) $R_{load} = 10 \Omega \rightarrow R_{load} = 0.55 \Omega$ with adaptive tuning. (c) $R_{load} = 0.55 \Omega \rightarrow R_{load} = 10 \Omega$ with a fixed compensator. (d) $R_{load} = 0.55 \Omega \rightarrow R_{load} = 10 \Omega$ with adaptive tuning. (e) $R_{load} = 0.55 \Omega \rightarrow R_{load} = 5 \Omega$ with a fixed compensator. (f) $R_{load} = 0.55 \Omega \rightarrow R_{load} = 5 \Omega$ with adaptive tuning.
the effect of a load transient from a sator given by (14) and the proposed adaptive tuning system where a comparison is made between the fixed PID compensator gain $K$ and the compensator zero locations $Z_1$ and $Z_2$ along with the measured stability margins $f_c$ and $\varphi_m$. The DCM compensator parameters have been tuned for $R_{load} = 5 \, \Omega$, while the CCM parameters have been tuned for $R_{load} = 0.55 \, \Omega$. Initially, there is a transient from $R_{load} = 5 \, \Omega$ to $R_{load} = 0.55 \, \Omega$, at which point, the parameters of the PID compensator are immediately switched to the previously tuned CCM values. After some time, another transient occurs from $R_{load} = 0.55 \, \Omega$ to $R_{load} = 10 \, \Omega$, which causes an error in measured versus desired stability margins, as shown in Fig. 8. Subsequently, the compensator parameters are retuned until zero error in the reference variables is again achieved.

VI. CONCLUSION

This paper has presented a method of continuous adaptive tuning of voltage-mode digital controllers for SMPS capable of automatically maintaining desired stability margins despite large signal transients from DCM to CCM and vice versa. A procedure, based on small-signal modeling, is used to significantly simplify the adaptive controller design. Simulation results are given showing that despite a wide range of uncertainty in the power stage, the adaptive tuner is still capable of maintaining the desired stability margins. The proposed adaptive tuning approach has been experimentally verified using a digitally controlled DCM/CCM buck converter as a test bed. The results indicate that by the use of the described adaptive tuning system, significant improvements in load transient performance are possible compared to a fixed control loop.

REFERENCES


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