An Online Phase Margin Monitor for Digitally Controlled Switched-Mode Power Supplies

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Abstract — This paper presents a practical injection-based method for continuous monitoring of the crossover frequency and phase margin in digitally controlled switched-mode power supplies (SMPS). The proposed approach is based on Middlebrook’s loop-gain measurement technique [1], adapted to digital controller implementation. A digital square-wave signal is injected in the loop, and the injection signal frequency is adjusted while monitoring loop signals to obtain the system crossover frequency and phase margin online, i.e., during normal SMPS operation. The approach does not require open loop or steady-state SMPS operation and is capable of convergence in the presence of load transients or other disturbances. Experimental results are presented for various power stage configurations demonstrating close matches between monitored and expected crossover frequencies and phase margins.

I. INTRODUCTION

Switching power converters are nonlinear systems with dynamic responses that depend on the operating point. Typically, based on averaged small-signal models, switched-mode power supply (SMPS) feedback loops are designed conservatively so that stability margins and closed-loop regulation performance are maintained over expected ranges of operating conditions and tolerances in power stage parameters. At design time, it is a common practice to measure the system loop gain using a network analyzer to verify the system stability margins under various conditions. Middlebrook’s injection technique [1] has been widely adopted in practice as it allows loop gain measurements without breaking the feedback loop. In this way, designs can be verified offline to ensure desired performance before system deployment.

With advances in digital control for high-frequency DC-DC converters [2], it becomes possible to consider alternative design approaches and techniques leading to improved closed-loop dynamic responses or improved robustness of SMPS. In particular, various methods have been proposed to measure converter frequency responses online [3-6] or to tune compensator parameters based on online assessments of the frequency responses [6-10]. In [3-5], a pseudo-random binary sequence perturbs the converter duty cycle for the purpose of identifying the open-loop control-to-output frequency response using cross-correlation methods. During duty-cycle perturbation, the system is temporarily operated in open-loop steady state. As a result, these approaches are best suited for one-time frequency response identification, e.g., upon start up, or at other times when the system is in steady state. In [6-11], frequency response information and tuning of compensator parameters is performed based on purposely induced limit-cycle oscillations in a sequence of steps, assuming steady-state operation.

In this paper, inspired by the analog injection technique [1], a method is proposed to measure the crossover frequency and phase margin in a digitally controlled power supply online, i.e., during normal system operation. The proposed approach does not require opening the feedback loop and is capable of continuously updating the measured crossover frequency and phase margin outputs in the presence of load transients or other system disturbances. Applications of the technique include fast design time verifications, online dynamic performance monitoring of power supplies in power distribution systems (such as servers or spacecrafts [12-14]), as well as adaptive online tuning of control parameters [15]. Section II details the proposed approach. Section III presents experimental results. Conclusions are given in Section IV.

II. STABILITY MARGIN MONITOR

Middlebrook’s analog loop gain measurement technique is a well known and widely accepted approach to measuring the loop frequency responses without breaking the feedback loop [1, 16]. Figure 1 illustrates this approach for the case of voltage injection \( V_z \) in series with the loop. The measured gain \( T_z(s) \) is

![Figure 1: Small-signal SMPS model illustrating analog loop gain measurement technique using voltage injection without breaking the feedback loop [1, 16].](image-url)
\[ T_v(s) = \frac{-V_y(s)}{V_x(s)} = T(s) \left( 1 + \frac{Z_1(s)}{Z_2(s)} \right) + \frac{Z_1(s)}{Z_2(s)}, \]  

where \( T(s) \) is the actual loop gain. Clearly, \( T(s) = T_v(s) \) as long as \( \|Z_\| \ll \|Z_2\| \) and \( \|T\| >> \|Z_1/Z_2\| \). In a SMPS with analog voltage-mode PWM control, points where the impedance conditions for the loop gain measurement using voltage injection are well satisfied typically include the converter output or the compensator output.

Figure 2 shows an implementation of the injection-based loop gain measurement technique applied to a digitally-controlled SMPS. The digital controller has the standard architecture including a voltage A/D converter (ADC), discrete-time compensator and digital pulse-width modulator (DPWM). Similar to the analog voltage injection approach, a small digital injection source \( V_z \) can be added to a digital loop signal at a suitable point. For example, injection can occur at the compensator input or at the compensator output, as shown in Fig. 2. It should be noted that a similar signal injection technique has been proposed for the purpose of tuning a compensator gain to achieve desired crossover frequency as part of an auto-tuning process [10].

Given the injection source \( V_z \) and the fact that \( \|Z_1/Z_2\| = 0 \) in the digital part of the loop, the system loop gain can be found as:

\[ T = -\frac{V_y}{V_x}. \]  

From (2), the crossover frequency, \( f_c \), can be found as the frequency where:

\[ T(e^{j\omega_c T}) = 1. \]  

while the phase margin is obtained from

\[ \varphi_m = 180\degree + \angle T(e^{j\omega_c T}) \bigg|_{\omega_c = 2\pi f_c}. \]

From (2) and (3), the crossover frequency \( f_c \) is equal to the injection source frequency,

\[ f_c = f_{inj}, \]

if

\[ \|V_z\| = \|V_x\|. \]  

Further, when (6) is satisfied, the phase margin can be directly measured as:

\[ \varphi = \varphi_m = \angle V_y(f_{inj}) - \angle V_x(f_{inj}). \]

Based on (2)-(7), the crossover frequency and phase margin can be monitored online in digitally controlled systems without requiring any additional power stage information. The monitoring can be performed continuously during normal operation of the system at the cost of a small output voltage perturbation imparted by the injection \( V_z \). However, the perturbation amplitude seen at the converter output can be automatically controlled by adjusting the signal injection amplitude \( \delta \), as shown in Fig. 2.

A more detailed block diagram of the stability margin monitor is shown in Fig. 3. Details regarding the design

![Figure 2: Crossover frequency and phase margin monitor block diagram. The outputs of stability margin monitor are crossover frequency and phase margin. The injection amplitude controller automatically adjusts the square-wave perturbation amplitude, \( \delta \), to result in minimum (+/- 1 LSB) perturbation at the output voltage.](image-url)
and implementation of each block in Fig. 3 are presented in the following subsections.

A. Injection Generator and Injection Amplitude Controller

The injection generator block creates a 50% duty cycle, square-wave perturbation with frequency adjustable by the frequency command, \( f_{\text{inj}} \). Practically, this square-wave signal can be generated with a digital counter, running off of a system clock having clock frequency \( f_{\text{clk}} \), and a simple comparator. The frequency resolution \( q_{\text{inj}} \) in \( f_{\text{inj}} \) depends on the ratio of the system crossover frequency \( f_c \) and the system clock frequency \( f_{\text{clk}} \);

\[
q_{\text{inj}} = \frac{f_c^2}{f_{\text{clk}}}.
\]  

In a typical system, the crossover frequency \( f_c \) is a fraction of the switching frequency \( f_s \), which, in turn, is a fraction of the system clock frequency. Hence, the resolution \( q_{\text{inj}} \) is typically a small fraction of \( f_c \).

To minimize the impact of the signal injection on the output voltage ripple, it is desirable to control the injection signal amplitude, \( \delta \), to obtain a minimum detectable +/-1 least significant bit (LSB) output voltage perturbation. However, in general the required injection signal amplitude, \( \delta \), is adjusted via feedback until the desired output voltage perturbation magnitude is achieved.

Figure 3: Blocks required to implement the stability margin monitor. The injection frequency is adjusted, via feedback, until the filtered peaks, \( ||V_x(f_{\text{inj}})|| \) and \( ||V_y(f_{\text{inj}})|| \) are equal. At this point, \( f_{\text{inj}} = f_c \) and \( \phi = \phi_m \).

Improved DC regulation, as explained in [17]. In particular, the +/- 1 LSB periodic oscillation imposed by \( V_z \) at the output voltage combined with the action of the integrator in the PID compensator will work to position the DC value of the output voltage in the center of the zero error bin. The accuracy with which the output voltage can be centered in the zero error bin then becomes a function of the DPWM resolution rather then the ADC resolution, which in general is finer to satisfy conventional limit cycle criteria [18, 19].

B. Band-pass Filters and Peak Detectors

As described previously, in the proposed implementation of Fig. 3, \( V_z \) is a 50% duty cycle square-wave injection with adjustable frequency determined by the frequency command \( f_{\text{inj}} \). However, (2)-(7) are based on the assumption that \( V_z \) is a purely sinusoidal injection. To account for the infinite odd harmonics introduced by the square-wave, band-pass filters are used to remove all unwanted frequency components of \( V_x \) and \( V_y \). The outputs of the band-pass filters, \( V_x(f_{\text{inj}}) \) and \( V_y(f_{\text{inj}}) \), then contain only one frequency component, equal to the injection frequency.

In Fig. 3, the band-pass filters, \( G_{bp}(z) \), are designed to be high Q-factor filters with the pass-band of the filter centered at \( f_{\text{inj}} \). However, since \( f_{\text{inj}} \) changes in order to satisfy (5), the filter pass-bands must also continuously change. To understand how to realize adjustable band-pass digital filters, consider a general form 2\(^{nd}\) order digital band-pass filter

\[
G_{bp}(z) = \frac{A - \frac{z - 1}{z^2 + Bz + C}}{z^2}. \tag{9}
\]

Based on the discrete-time to continuous-time mapping

\[
\frac{s}{z} = e^{j\omega_{\text{sample}}}, \tag{10}
\]

the pass-band center frequency \( f_{pb} \) and the Q-factor of (9) can be found as

\[
f_{pb} = \frac{f_{\text{sample}}}{2\pi} \tan^{-1} \left( \frac{\sqrt{B^2 - 4C}}{B} \right), \tag{11}
\]

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Given $f_{\text{sample}}$, $f_{\text{finj}}$, and $Q$, (11) and (12) can be used to solve for the filter coefficients $B$ and $C$. Then, by holding $A$, $B$, and $C$ constant while varying $f_{\text{sample}}$ in proportion to $f_{\text{finj}}$, the filter pass-band center frequency $f_{\text{fb}}$ shifts in proportion to $f_{\text{finj}}$ while $Q$ stays constant.

The peak detectors take as inputs the filtered waveforms, $V_x(f_{\text{finj}})$ and $V_y(f_{\text{finj}})$, and output $||V_x(f_{\text{finj}})||$ and $||V_y(f_{\text{finj}})||$, as shown in Fig. 3. The peak detectors give an assessment of the magnitudes of each signal such that (6) can be satisfied by closing an integral feedback loop around the injection frequency.

### C. Integral Compensator

A slow integral compensator is used to process the error between $||V_x(f_{\text{finj}})||$ and $||V_y(f_{\text{finj}})||$. Since the stability margin monitor control loop is a sampled-system, its bandwidth must be much slower than the injection frequency (which upon convergence equals $f_c$). Therefore, a slow integral compensator is sufficient to close the feedback loop in the stability margin monitor. The output of the integral compensator is $f_{\text{finj}}$, the injection frequency command, which is adjusted until there is no error between $||V_x(f_{\text{finj}})||$ and $||V_y(f_{\text{finj}})||$, at which point (6) is satisfied and $f_c = f_{\text{finj}}$.

### D. Phase Detector

The phase detector block diagram, used to monitor $\varphi_{\text{net}}$, is shown in Fig. 5 and is similar to some approaches used to detect phase in digital phase-locked loops [20]. The phase detector takes as input the filtered signals, $V_x(f_{\text{finj}})$ and $V_y(f_{\text{finj}})$. These signals are passed through a digital relay whose output is high when the input is above zero and low when the input is below zero. The two relay outputs are then XOR’d together to form an Enable pulse, labeled in Fig. 5, which is high when the two inputs are not equal. This enable pulse gives a direct relationship between the phases of the two inputs signals. A counter running at the system clock frequency, $f_{\text{clk}}$, measures the length of time Enable is high which is related to the phase shift between $V_x(f_{\text{finj}})$ and $V_y(f_{\text{finj}})$.

There are two important sampling effects which determine the resolution of the phase detector. First, the system clock frequency determines the resolution in degrees in the detected phase,

$$q_{\text{PM}} = 360\varphi/\gamma.$$  \hfill (13)

Since $f_c$ is typically a fraction of the switching frequency, which is a fraction of the system clock frequency, (13) implies a phase detection resolution of several degrees.

The other main factor in the resolution/accuracy of the phase detector is the sample rate, $f_{\text{sample}}$, of the band-pass filters with respect to $f_{\text{finj}}$

$$f_{\text{sample}} = \gamma f_{\text{finj}}.$$  \hfill (14)

where $\gamma$ is an integer proportionality constant. Since $V_x(f_{\text{finj}})$ and $V_y(f_{\text{finj}})$ are sampled at a rate proportional to $f_{\text{finj}}$, their respective zero crossings could be shifted by as much as one sample period, $1/f_{\text{sample}}$, from the actual zero-crossings. Therefore, the phase error satisfies

$$\text{PM error} \leq \frac{360\varphi}{\gamma}.$$  \hfill (15)

As $\gamma$ is increased, (15) approaches zero and the phase margin resolution is dominated by (13). Note that (15) gives the maximum phase error (i.e. the phase error is guaranteed to be no larger than (15)).

### III. Experimental Results

There are two experimental test-beds, shown in Fig. 6, used to verify functionality of the proposed stability margin monitor, a synchronous buck converter and a boost converter which can be operated in continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

![Figure 5: Block diagram of the phase detector. A system clock, $Clk$, is used to measure the time shift between $V_x(f_{\text{finj}})$ and $V_y(f_{\text{finj}})$.](image)

![Figure 6: Experimental prototypes used for testing stability monitor (a) Synchronous buck converter, (b) CCM or DCM boost converter.](image)
The nominal power stage parameters of the buck converter are given in Fig. 6(a). The buck converter output voltage ADC is a TI-THS1030 with an effective output voltage LSB resolution of 20 mV. The nominal switching frequency is 100 kHz.

Nominally, the boost converter power stage parameters are as shown in Fig. 6(b) with \( V_g \) and \( L \) depending on the mode of operation (CCM or DCM). In CCM, \( V_g_{CCM} = 15V \) and \( L_{CCM} = 100 \mu H \). In DCM, \( V_g_{DCM} = 10V \) and \( L_{DCM} = 20 \mu H \). The boost converter ADC is an AD7822 with an effective output voltage resolution of 512 mV. As with the buck converter, the nominal switching frequency is 100 kHz.

In all power stages, the system clock frequency is \( f_{clk} = 50 MHz \), which from (13) implies

\[
q_{PM} = \frac{360^\circ}{\frac{f_c}{50MHz}} = \frac{7.2 \times 10^{-6}}{f_c}. \quad (16)
\]

The matched band-pass filters were implemented using the following transfer function

\[
G_{bp}(z) = 0.00195 \frac{z-1}{z^2 + 1.989z - 0.998}. \quad (17)
\]

Where \( f_{sample} = 32 f_{nor} \), i.e., \( \gamma = 32 \). Based on (11) and (12), the filter pass-band center frequency and Q-factor are

\[
f_{pb} = \frac{f_{sample}}{32}, \quad \text{and} \quad Q = 100 = 40dB. \quad (18)
\]

Further, from (15) and (18), the maximum possible phase error expected in hardware is

\[
PM_{error} \leq \frac{360^\circ}{32} = 11.25^\circ. \quad (20)
\]

The input injection magnitude, \( \delta \), is continuously updated based on the injection amplitude controller shown in Fig. 4 until the output voltage error \( V_{err}[n] \) is minimum possible, +/- 1 LSB. In the experimental prototypes, this amounts to +/- 0.4% output voltage perturbation in the buck converter and +/- 1.6% perturbation in the boost converter. The speed of the input amplitude controller has been designed to be faster than the monitoring control loop.

Given the described experimental systems, Table I summarizes the experimental performance of the stability margin monitor with four different power stage configurations. In Table I, \( f_{nor} \) and \( \phi_m \) based on the proposed monitoring approach closely match the expected values for each case, based on the discrete-time model of [21]. Further, the monitored phase margin never deviates more than 11.25° from the predicted value, thus satisfying the expected error given by (20). Note that the phase margin results given in Table I are averaged

<table>
<thead>
<tr>
<th>System</th>
<th>Converter</th>
<th>G_c(z)</th>
<th>Analytical Stability Margins</th>
<th>Digital Stability Margin Detection</th>
<th>Analog Injection Results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Analytical ( f_c )</td>
<td>Analytical ( \phi_m )</td>
<td>Measured ( f_c )</td>
</tr>
<tr>
<td>System 1</td>
<td>Buck Converter</td>
<td>( \frac{(z - 0.762)(z - 0.91)}{(z + 0.4)(z - 1)} )</td>
<td>9.22 kHz</td>
<td>55.0°</td>
<td>9.20 kHz</td>
</tr>
<tr>
<td>System 2</td>
<td>Buck Converter</td>
<td>( \frac{(z - 0.83)(z - 0.728)}{(z - 1)} )</td>
<td>13.8 kHz</td>
<td>27°</td>
<td>13.89 kHz</td>
</tr>
<tr>
<td>System 3</td>
<td>CCM Boost Converter</td>
<td>0.035 ( \frac{2}{z - 1} )</td>
<td>1.20 kHz</td>
<td>85.1°</td>
<td>1.23 kHz</td>
</tr>
<tr>
<td>System 4</td>
<td>DCM Boost Converter</td>
<td>( \frac{2.0(z - 0.8)}{(z - 1)} )</td>
<td>6.87 kHz</td>
<td>65.6°</td>
<td>6.42 kHz</td>
</tr>
</tbody>
</table>

The experimentally observed dynamic performance of the stability margin monitoring control loop. The dynamic response to a change from \( V_f = 12V \) to \( V_f = 8V \) with the compensator of System 1: (a) crossover frequency \( f_c \), (b) Phase margin \( \phi_m \) with maximum expected phase error based on (20), (c) Injection amplitude \( \delta \).
over 100 samples. Table I also shows measured results based on the standard analog injection technique, obtained by introducing an analog voltage injection, $V_z$, at the converter output (Point A in Fig. 6), with the digital stability monitor disabled. The results from the standard analog injection technique indicate close matches with the measurements from the proposed digital technique and the discrete-time model. Based on the cases tested in Table I, worst case injection frequency and phase margin resolution can be determined from (8) and (13). Based on the highest crossover frequency for the tested systems, the injection frequency resolution is always greater than 4 Hz while the phase margin resolution is always greater than 0.1°.

Figure 7 shows the experimentally observed dynamics of $f_{int}$, $q_m$, and $\delta$, captured in Chipscope (a Xilinx embedded FPGA logic analyzer), under a power stage line transient. In particular, Fig. 7(a), Fig. 7(b) and Fig. 7(c) show a bus voltage change in the synchronous buck converter power stage from 12V to 8V with the compensator of System 1. Under this change, the monitor recognizes the bus voltage change and updates the outputs accordingly. The high frequency noise seen in the monitored phase margin is an artifact of the band-pass filter sample rate selection discussed previously. Note however that the magnitude of the high frequency noise is always less than the error predicted by (20), as expected.

One advantage to the proposed solution to monitoring stability margins is that the system does not require open loop or steady-state operation. This allows the monitor to run and converge despite power stage transients (load, line, etc.). Figure 8 shows the load transient response of System 1 of Table I (buck converter) and System 4 of Table I (DCM boost converter) with and without the stability margin monitor. First, Fig. 8(a) is the load transient response, from 2.5A to 0A, of System 1 without the phase margin monitor. As expected, the load transient causes a deviation in output voltage, which returns to steady state after some time due to the action of the feedback loop. In Fig. 8(c), the same load transient is imposed as in Fig. 8(a), but with the stability margin monitor.
monitor control loop running. Note the oscillation imposed by $V_i$ is only +/- 1 LSB due to the action of the feedback loop controlling $\delta$. Also, note that the frequency of $V_i$ is equal to the crossover frequency. Load transient results are presented in Fig. 8(b) and Fig. 8(d) for System 4 of Table I, the DCM boost converter. Since the boost converter is operating in DCM, the load transient (from 3A to 50mA) significantly affects the crossover frequency, as indicated by the oscillation frequency before and after the transient in Fig. 8(d). Based on the discrete-time model [21], the expected crossover frequency after the load transient is 4.1 kHz, which is approximately the frequency of oscillation seen in Fig. 8(d).

In Fig. 8(c) and Fig. 8(d), notice the output voltage perturbation combined with the action of the integrator in the PID compensator centers the DC value of the output voltage in the zero error bin with accuracy related to the DPWM resolution rather than the ADC resolution, as discussed previously. Since in general the DPWM resolution is finer than the ADC resolution, this equates to more precise DC regulation accuracy with the imposed output voltage oscillation than without.

As a final note, the hardware required to implement all of the above described blocks is summarized in Table II. As indicated, to implement the entire stability margin monitor requires a relatively modest gate count and no additional memory.

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>REQUIRED LOGIC RESOURCES TO IMPLEMENT DIGITAL STABILITY MONITOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>Logic Gates</td>
</tr>
<tr>
<td>Injection/Clock Generator</td>
<td>1262</td>
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<tr>
<td>Band-pass Filters</td>
<td>2288</td>
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<tr>
<td>Peak Detectors</td>
<td>1230</td>
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<tr>
<td>Integral Compensator</td>
<td>1034</td>
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<tr>
<td>Amplitude Controller</td>
<td>1448</td>
</tr>
<tr>
<td>Total</td>
<td>7252</td>
</tr>
</tbody>
</table>

III. CONCLUSIONS

This paper presents a practical method for continuously monitoring the crossover frequency and phase margin in digitally controlled switching power converters. The proposed approach does not require open loop operation and is capable of converging to correct results in the presence of load transients or other disturbances. Further, the stability margin monitoring requires and ensures that only +/- 1 LSB output voltage perturbation is caused by the monitor. Experimental results are presented for four different system configurations indicating close matches between monitored and expected crossover frequencies and phase margins. Experimental results are also presented showing the observed output voltage and inductor current during a load transient, indicating that the control loop is unaffected by disturbances.

REFERENCES