Abstract—This paper introduces modular masterless multi-phase architecture based on identical digitally controlled DC-DC converter modules that communicate over a digital bus. Advantages of the masterless architecture include simpler system configuration and development, and scalability to an arbitrary number of phases. Technical challenges are to facilitate proper phasing, control and current sharing functions, while minimizing data throughput requirements for the digital bus. A chain control algorithm is proposed to implement current sharing control in the modular masterless architecture. The algorithm performs a moving window averaging with relatively low storage and communication requirements. Implementations of the chain control in current-mode control systems and voltage-mode control systems are described in this paper. Experimental results are presented for a two-phase 12-V to 1.5-V, 15-A synchronous buck converter with digital voltage-mode control.

I. INTRODUCTION

Power supplies for high performance microprocessors must deliver low supply voltages with high currents while maintaining tight output voltage regulation in the presence of large load transients. Interleaved multi-phase converters are frequently used in such systems due to many advantages such as total current division among the phases, lower switching frequency for each phase, fast transient response, as well as reduced switching ripples in the input current, the output current and the output voltage.

In general, multi-phase converters require additional circuitry to ensure appropriate current sharing among the phases. In multi-phase systems, a current imbalance is a result of power stage component tolerances, variations caused by environmental conditions, and non-identical connections from the converters to the shared load. Additionally, variations in compensator parameters, turn on/off times of power MOSFETs and interconnection delays also result in uneven current distribution among the phases. The current imbalance may result in increased current or thermal stresses on the components.

A number of current sharing approaches have been proposed in the literature [1-21], including passive and active methods using analog or digital controllers. In most cases, to facilitate proper phasing, control or current sharing functions, the controller for a multi-phase system includes a dedicated master.

The purpose of this paper is to introduce a modular masterless multi-phase architecture [22], as shown in Fig. 1, and develop a current sharing approach suitable for such a system. The proposed masterless multi-phase architecture is based on identical digitally controlled DC-DC converter modules that communicate over a digital bus. A similar architecture has been proposed in [21]. Advantages of the masterless architecture include simpler system configuration and development, scalability to an arbitrary number of phases, redundancy and potentials for improved reliability and reduced system cost based on identical modules.

An overview of current sharing methods in the literature is given in Section II. Section III discusses technical issues in the modular masterless multi-phase architecture. The proposed current-sharing method, which is called the “chain control” algorithm, is introduced in Section IV. Implementations of the chain control in modules with current-mode control and voltage-mode control are discussed in Sections V and VI, respectively, together with simulation results. Section VII presents experimental verification on a two-phase 12-V to 1.5-V synchronous buck converter with digital voltage-mode control.

II. OVERVIEW OF CURRENT SHARING APPROACHES

This section presents a summary of analog and digital current sharing methods reported in literature [1-21].

A. Analog current sharing methods

A variety of analog approaches to current sharing have been
proposed, analyzed and developed covering a wide range of complexities and current sharing performance [1-16].

Among these methods, droop current sharing methods are among the simplest [1-4] because they are based on passive current sharing without the need for feedback control or communication among the phases. However, droop methods have a drawback of poor load regulation, so they are not suitable for high performance applications.

Active current sharing methods employ feedback control to achieve improved current sharing performance, at the expense of more complex sensing and control circuitry. In active control methods, the current of each phase is regulated to be equal to a “reference” current. Current sharing control strategies differ in how they define the reference current, including:

1) using current of a specific phase as the reference, such as master-slave methods with a dedicated master [1-3, 6];
2) using the maximum [1-3, 6-8] or the minimum [9] current among all phases as the reference, such as master-slave method with an automatic master;
3) using the average current (or weighed average) of all phases as the reference [1,2, 10-16]. The average current can be obtained by a single current sharing wire, commonly referred to as ‘democratic’, ‘autonomous’ or ‘single wire’ methods [10-16]. The average current or the weighed average can also be obtained by an external controller, as in “central limit” methods [1, 2 and 6].

Among these methods, automatic master-slave methods and democratic average current methods have the best modularity: the system operation does not depend on a specific phase, a sensing point, or an external controller.

After the reference current is defined, inductor currents of each phase can be regulated to follow the reference. As a result, the load current can be shared evenly among the phases. Current regulation can be performed in both voltage mode control systems and current mode control systems.

B. Digital current sharing methods

Digital controllers are strong candidates for microprocessor power supplies due to their inherent design and operating flexibility [17-23]. Digital approaches have the ability to implement more complicated or advanced control schemes and support reconfigurable and adaptive functions. The design can be easily adapted to different technologies or modified to meet a different application or a new set of specifications. Digital compensators and control logic are also relatively immune to process and environmental variations, allowing designs to be optimized for high performance rather than for worst-case conditions.

A digital passive current sharing approach was described in [17]. The current sharing is based on digital PWM techniques that result in perfect matching of duty cycles of PWM signals among different modules. The approach is well suited to applications using a single master controller with tight matching of gate driver delays and power stage components among the phases.

Active current sharing methods are employed in [18-20]. In [20], a digital master controller is used to average the sensed currents and provides control to all the phases.

The concept and implementation of the reported digital current sharing techniques are relatively simple in a system with a master controller, as shown in Fig. 2.

The master-based approach requires dedicated connections between the master controller and a slave controller for each phase, including voltage sensing, current sensing and gate drive signals, which impacts noise coupling and reliability as well as system size and cost. This limitation will become increasingly important in future microprocessor power supplies, where the rapidly increasing supply current requirements are expected to drive the number of required phases up. This provides a motivation for exploration of alternative masterless multi-phase architecture with improved scalability to an arbitrary number of phases.

III. MODULAR MASTERLESS MULTI-PHASE ARCHITECTURE

Modular masterless multi-phase architecture based on identical digitally controlled DC-DC converter modules that communicate over a single digital bus is proposed in this paper, as shown in Fig. 1.

The identical converter modules are connected in parallel to supply load current in a phase-shifted manner. The use of all identical modules makes the system simple to configure, develop and scale. Ideally, only the shared communication bus and input/output power traces are built on board and allow an arbitrary number of converter modules to be connected. This leads to good redundancy and a potential for improved reliability as well as the ability to deploy the system easily according to total load requirements.

A design goal for the converter modules in the system of Fig. 1 is that they should be able to operate individually and in coordination with an arbitrary number of other modules. Each converter module is composed of a power stage (DC-DC converter), a digital controller, and analog to digital interface components (A/Ds and/or D/As). A digital communication bus is employed to share information for interleaved operation and current sharing.

The digital controller performs voltage regulation, current sharing control, communication interface to the digital bus and/or digital pulse width modulation, together with other functions such as automatic phase-shifted operation, output voltage positioning, and re-configurability (e.g. programmable output voltage or droop rate).
Compared to a digital master controller design, there are additional challenges in the design of such identical distributed digital controllers in the masterless architecture. Since each controller performs exactly the same functionality and has access only to its own voltage/current information and the common digital bus, special algorithms are needed to implement interleaved operation and current sharing while minimizing the communication and processing requirements. This paper focuses on the challenges of current sharing control in the masterless system.

IV. CHAIN CONTROL ALGORITHM

This section introduces the chain control algorithm for communicating the current sharing information among identical phases over a digital bus. It is desired to find the average current as the current reference. With a digital master controller, this can be achieved simply by gathering current information from all phases, computing the average value and adjusting control outputs to all phases so that the current in each phase follows the computed average.

In the masterless architecture, each phase operates independently and executes exactly the same control algorithm in a phase-shifted manner. The challenge is to provide the necessary information for each phase to determine the average current in both steady state and transients, while minimizing the communication data rate, processing and date storage overheads.

One way to compute the average current is proposed in [21]. A Control Area Network (CAN) interface card is used in each module, and a packet of data is broadcast periodically by each module. So in an N-phase system, each module needs to receive data (N-1) times and computes the required values N times per switching cycle. For current averaging, N sensed currents need to be stored in a memory. Here, we propose an approach with reduced storage and communication requirements.

The chain control algorithm is designed to perform a moving window average for current sharing in the masterless architecture. In an N-phase interleaved multi-phase system, one switching period can be divided into N slots, each allotted to a single phase. For trailing edge modulation, each phase generates a rising edge on its PWM modulation signal at the beginning of its allotted slot. The falling edge is determined by the duty cycle command generated by the digital controller in that phase. Since only one duty cycle command is executed in each switching period, the phase current information and the computed reference current are only needed during the allotted slot for each phase. With the chain control algorithm, each phase computes the average current only once per switching period.

To explain the chain control algorithm, we take a 4-phase system as an example. The interleaved four phases operate in sequence, so in the n\textsuperscript{th} switching cycle, the currents of each phase, $I\textsuperscript{[1]}[n]$, $I\textsuperscript{[2]}[n]$, $I\textsuperscript{[3]}[n]$, and $I\textsuperscript{[4]}[n]$ are obtained in sequence. The objective is to find the average value of the newest four currents at any given time. For example, the average current computed by Phase 1 in the n\textsuperscript{th} switching cycle is

$$I\text{ave}[1] = \frac{(I\textsuperscript{[1]}[n-1] + I\textsuperscript{[3]}[n-1] + I\textsuperscript{[4]}[n-1] + I\textsuperscript{[1]}[n])}{4}, \quad (1)$$

where $I\textsuperscript{[1]}[n]$ is the current of phase 1 obtained in the switching cycle n, and $I\textsuperscript{[2]}[n-1]$, $I\textsuperscript{[3]}[n-1]$, $I\textsuperscript{[4]}[n-1]$ are the currents of the other 3 phases obtained in the previous switching cycle (n-1). Similarly, for the next phase, the computed average current is

$$I\text{ave}[2] = \frac{(I\textsuperscript{[3]}[n-1] + I\textsuperscript{[4]}[n-1] + I\textsuperscript{[1]}[n] + I\textsuperscript{[2]}[n])}{4}. \quad (2)$$

Comparing (1) and (2), we obtain

$$I\text{ave}[2] = I\text{ave}[1] - I\textsuperscript{[2]}[n-1]/4 + I\textsuperscript{[2]}[n]/4. \quad (3)$$

Equation (3) leads to the concept of chain control. In an N-phase system, the contribution of phase i in the average current is $I[i]/N$. If each phase could obtain the average current computed by the previous phase, then subtract its old contribution $I[i][n-1]/N$ and add the new contribution $I[i][n]/N$, it will have an updated average current value.

In all, the chain control performs a moving-window averaging and is described by

$$I\text{ave}[i] = I\text{ave}_{prev} - I[i][n-1]/N + I[i][n]/N, \quad (4)$$

where $I\text{ave}_{prev}$ is the average current computed by the previous phase. The chain control averaging described in (4) is well suited for digital implementation, as shown in Fig. 3.

![Fig. 3: Digital implementation of the chain control algorithm](image-url)

In a masterless multi-phase system, each phase reads $I\text{ave}_{prev}$ from the digital bus, performs the computation as in (4), and drives the current-sharing bus with the updated average current $I\text{ave}$ once per switching cycle. As a result, the average current value is updated in sequence all the time.

Note that with this method, only one variable, $I[i][n-1]$, needs to be stored in each phase, regardless of the total number of phases in the system. All variables are “local” (obtained inside this phase), except $I\text{ave}_{prev}$ so each phase only needs to read from the digital bus once and compute the average current once per switching cycle. If N is a power of 2, the multiplier can be replaced by a shift register. The hardware to implement (4) can be very small.

The computed average current by the chain control algorithm can be used in different ways depending on the closed-loop control method. If the system has an analog current mode controller together with a digital controller for
voltage regulation, the digital current command is averaged to implement current sharing, which is discussed in Section V. For modules based on digital voltage mode control, the error between the sensed current and the computed average current can be included in the voltage loop compensator design, as discussed in Section VI.

V. CHAIN CONTROL IN CURRENT MODE CONTROL SYSTEMS

The proposed current sharing method can be combined with any current mode control approach. As an example, consider analog peak (or average) current mode control in combination with digital voltage-loop compensation, as shown in Fig. 4. The digital voltage-loop compensator takes the output voltage error as the input and computes the digital current command $I_{\text{calc}}$. In peak (or average) current mode control without current sharing, the calculated $I_{\text{calc}}$ is used as the current command $I_c$ to control the sensed peak (or average) inductor currents.

To implement the chain control current sharing in this system, (4) is used to find the average of the calculated current commands, as shown in Fig. 5. Then the module asserts the computed average value on the shared digital bus, and also uses this value as the current command $I_c$ for the current-mode controller. In this manner, all phases share the same peak (or average) current.

A two-phase system composed of two of the modules shown in Fig. 5 is validated by simulation (Matlab, Simulink) using 12 V-to-1.5 V buck converters operating at 100 kHz switching frequency. A mismatch is created in the two power stages by giving different parasitic resistances for the inductors: Phase 1 has $R_L = 5 \, \text{m} \Omega$ and Phase 2 has $R_L = 2.5 \, \text{m} \Omega$. The system is tested under a load transient from 25 A to 50 A. Without chain control, the two current are different because of different open-loop control-to-current DC gains, as shown in Fig. 6 (a). With chain control, the two inductor currents are controlled to be the same before and after the load transient, as shown in Fig. 6 (b).

It is noticed that the averaging effect of chain control affects the transient current responses. During a large transient, fast inductor current changes are desired. With chain control, steps of transient current commands are also averaged, slowing the transient response slightly compared to the operation without chain control. This leads to slightly larger overshoots and undershoots in the current response and directly affects the output voltage transient.

To solve this problem, the ideal behavior of the chain control algorithm is to make current commands all equal to the average value during steady state operation, while allowing individual phase current command steps during large transients. To realize this modification, an additional filter is applied to the current command computation, as

$$I_c[i][n] = I_{\text{ave}}[i][n] + (I_{\text{calc}}[i][n] - I_{\text{ave}}[i][n]) \cdot (\text{Filter}) \cdot (5)$$

The behavior of the filter is that when there is a step change in the input $(I_{\text{calc}}[i][n] - I_{\text{ave}}[i][n])$, the first step of the filter output is equal to the input step, then decays to zero after a number of samples. In steady state operation, $I_{\text{calc}}$ is equal to $I_{\text{ave}}$. When there is a large transient, $I_{\text{calc}}$ will have a step change, so does $(I_{\text{calc}} - I_{\text{ave}})$. At the first step of the transient, $I_c[i][n] = I_{\text{ave}}[i][n] + (I_{\text{calc}}[i][n] - I_{\text{ave}}[i][n]) \cdot 1 = I_{\text{calc}}[i][n] \cdot (6)$

which allows individual phases to pass transient current step commands immediately when sensed. In steady state,

$$I_c[i][n] = I_{\text{ave}}[i][n] + (I_{\text{calc}}[i][n] - I_{\text{ave}}[i][n]) \cdot 0 = I_{\text{ave}}[i][n] \cdot (7)$$
which results in the same steady-state current sharing performance as (4).

Simulations have been performed in a 4-phase system to validate the transient improvement. Four buck converter modules with peak current mode control are connected in parallel. A mismatch among the phases is modeled in the voltage loop compensators by giving a gain of 1.2 to two of the phases and 0.8 to the other two phases. Figure 7 shows the result of a load transient with and without chain control prior to applying the transient improvement filter.

In Fig. 7 (a), without current sharing chain control, there are no voltage undershoots during transients, but the load current is not shared evenly in steady state. Figure 7 (b) shows the transient result when using chain control, as in Fig. 5, where load currents are shared in steady state, but there is undershoot in the output voltage because of the averaged inductor current steps.

Figure 8 shows the digital implementation of chain control (4) with transient improvement (5) and a discrete-time filter. Figure 9 shows the simulation results for this system. We can see that during the load transient, the inductor currents of individual phases respond immediately with large steps similar to the case without current sharing and do not result in an additional voltage undershoot. In steady state, the inductor currents are shared equally, as in the case of Fig. 7 (b).

VI. CHAIN CONTROL IN VOLTAGE MODE CONTROL SYSTEM

In a digital voltage mode control system, the digital controller takes the output voltage error as the input and computes a digital duty cycle command for the digital pulse width modulator (DPWM) to control the power stage, as shown in Fig. 10 [22, 23].

Without current sharing control, there is no mechanism to ensure current sharing in the presence of module mismatches. An increase (or decrease) in duty cycle command of one phase can result in current increasing (or decreasing) in this phase.

To realize current sharing, the inductor currents are sensed and the chain control is used to compute the average of the sensed inductor currents, as shown in Fig. 11. A current error is generated by comparing the updated average current computed by (4) and the sensed current, and applied to the voltage and current compensator to realize inductor current sharing.

The voltage and current compensator combines the effects of the voltage error and the current error:

\[ d[n] = d[n-1] + f(v_{\text{error}}) + g(i_{\text{error}}). \]  

(8)

The functions \( f(v_{\text{error}}) \) and \( g(i_{\text{error}}) \) include design parameters that can be programmed for different applications. In the work reported in this paper, we have:

\[ d[n] = d[n-1] + f(v_{\text{error}}) + g(i_{\text{error}}). \]  

(8)
\[ f(\text{error}) = a_1 \cdot \text{error}[n] + a_2 \cdot \text{error}[n-1] + a_3 \cdot \text{error}[n-2] \]
\[ g(\text{error}) = b \cdot i_{\text{error}}[n] \] (9)

In microprocessor power supplies, fast voltage regulation is always required to minimize transient voltage overshoots or undershoots. The current sharing performance is particularly important in steady-state operation. To simplify compensator design, the voltage regulation loop is designed to be much faster than the current regulation loop by setting \( a_1 \gg b \). When the voltage error is not zero, the \( \text{error} \) terms are dominant, and the compensator is essentially a voltage loop PID compensator. When the voltage error is regulated to be small, the compensator becomes a current loop PI compensator.

A two-phase system composed of two of the modules shown in Fig. 11 is used for validation by simulation. Power stages are 12 V to 1.5 V buck converters operating at 100 kHz switching frequency. A mismatch between the stages is modeled by setting different parasitic resistances for the inductors: Phase 1 has \( R_L = 5 \text{ m}\Omega \) and Phase 2 has \( R_L = 2.5 \text{ m}\Omega \). The load transient is from 25 A to 50 A. Simulation results are shown in Fig. 12. With chain control, the two inductor currents converge to the same value in steady state, as shown in Fig. 12 (b).

Note that since the current sharing loop is designed to be much slower than the voltage regulation loop, during large load transient, the compensator behaves essentially the same as without current sharing, removing the need for the transient improvement filter discussed in Section V.

A field programmable gate array (FPGA) based digital controller using a Xilinx Virtex II evaluation board is used to implement the functionality of the two digital controllers and the communication between them. Analog-to-digital converters (THS1230) are used to convert the sensed voltage errors and inductor currents to digital signals. Current sensing is based on sensing the voltage across \( R_{on} \) of the synchronous rectifier. Further details of the experimental test circuit can be found in [24]. Digital voltage errors and the inductor currents are used for voltage regulation and current sharing control.

Figure 14 shows the experimental result before and after the chain control is enabled when the load current is 8 A. The upper signal is the chain control enable signal and the lower two signals are the two inductor currents. Before chain control is enabled, the two inductor currents are different due to mismatches in the power stages (mainly the non-identical connections between the converter outputs to the load). The two currents are then gradually regulated to be identical following activation of the chain control current sharing.

It was observed that at some current levels the current regulation loop exhibited small limit cycle oscillations. To address this problem, a windowed current regulation approach was applied and tested. When the current errors have been inside a given window for a number of cycles (40 switching cycles in our implementation), the current sharing control is disabled by setting \( b = 0 \) in (9). When the current error exceeds the regulation window, the current sharing control is enabled immediately.

Fig. 13: Experimental system setup: a two-phase masterless system consisting of two identical synchronous buck converters controlled by two identical digital controllers.

Fig. 14: Experimental results in the voltage-mode controlled two-phase buck converter, before and after chain control current sharing is enabled. Upper: chain control enable signal; lower: two inductor currents
Figure 15 (a) shows current sharing performance without the windowed current regulation. We can see that the currents have small variations in steady state, indicating the presence of limit-cycle oscillations. With the windowed current regulation (window size: ±2LSB = ±0.34 A), the current regulation loop is open in steady state, so there is no current loop limit cycling, as shown in Fig. 15 (b). However, a small steady state error appears between the two currents due to the size of the regulation window. The choice of the window size is dictated by the current sharing requirements.

![Fig. 15: Experimental results for the voltage-mode controlled two phase buck converter with the chain control current sharing: (a) without and (b) with windowed current regulation. Upper: load control signal, lower: two inductor currents](image)

VIII. CONCLUSIONS

This paper introduces a modular masterless multi-phase architecture based on identical digitally controlled DC-DC converter modules that communicate over a digital bus. Advantages of the masterless architecture include simpler system configuration and development, and scalability to an arbitrary number of phases. Technical challenges are to facilitate proper phasing, control and current sharing functions, while minimizing data throughput requirements for the digital bus.

The paper describes a chain control algorithm to implement current sharing control in the modular masterless architecture. The chain control algorithm performs a moving window averaging with minimized storage and communication requirements to compute the current reference in each phase. Implementations of the chain control in current-mode control systems and voltage voltage-mode control systems are described. Experimental results with a two-phase 12-V to 1.5-V 15-A synchronous buck converter with digital voltage-mode control demonstrate functionality of the chain control current sharing.

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