Design and Implementation of an Adaptive Tuning System Based on Desired Phase Margin for Digitally Controlled DC–DC Converters

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Abstract—This letter presents an online adaptive tuning technique for digitally controlled switched-mode power supplies (SMPS). The approach is based on continuous monitoring of the system crossover frequency and phase margin, followed by a multi-input–multi-output (MIMO) control loop that continuously and concurrently tunes the compensator parameters to meet crossover frequency and phase margin targets. Continuous stability margin monitoring is achieved by injecting a small digital square-wave signal between the digital compensator and the digital pulsewidth modulator. The MIMO loop adaptively adjusts the compensator parameters to minimize the error between the desired and measured crossover frequency and phase margin. Small-signal models are derived, and the MIMO control loop is designed to achieve stability and performance over a wide range of operating conditions. Using modest hardware resources, the proposed approach enables adaptive tuning during normal SMPS operation. Experimental results demonstrating system functionality are presented for a synchronous buck SMPS.

Index Terms—Adaptive control, dc–dc power conversion, digital control.

I. INTRODUCTION

WITHCHED-MODE power supply (SMPS) feedback loops are typically designed conservatively so that closed-loop regulation and stability margins are maintained over expected ranges of operating conditions and tolerances in power stage parameters. Typical designs often lead to degraded closed-loop performance or loss of stability in the event of significant operating point changes associated with component degradation, input voltage variations, etc. These types of power stage parameter changes are mitigated by offline controller redesign to maintain desired dynamic performance requirements. With the increased feasibility of practical digital control in switching power converters [1], new opportunities exist to incorporate intelligent control algorithms into the system to improve dynamic responses and reliability over a wider range of possible operating points.

Recent work in the area of digital control of dc–dc power converters has shown that autotuning algorithms can be completely integrated into the digital controller with relatively small additional hardware requirements [2]–[8]. In particular, approaches to onetime compensator autotuning based on frequency response data, gathered online, have been proposed in [2]–[8]. However, the identification of frequency-response information requires more significant signal processing [2]–[4], or several tuning steps [5]–[7], and assumes undisturbed, steady-state operation. The tuning approach proposed in [8], which is capable of operation during load transients, also proceeds in two predefined steps. For these reasons, it is more difficult to apply [2]–[8] directly to continuous parameter tuning.

The goal of this letter is to present an approach, based on a large body of work in adaptive control theory [9]–[12], to adaptive tuning of digital SMPS controller parameters during normal closed-loop operation of the converter. The proposed approach is similar in objectives to the work presented in [13], but the method in which compensator tuning is performed is very different. The proposed approach is based on continuous monitoring of the system crossover frequency and phase margin [14], and a multi-input–multi-output (MIMO) control loop that adaptively tunes the compensator parameters to meet crossover frequency and phase margin targets. Similar to [8], a digital signal injection is introduced while the converter operates in closed loop. However, in contrast to [8], this approach tunes all parameters of the compensator continuously and concurrently. Further, the adaptive tuning causes a very small output voltage perturbation thus allowing tuning without disturbing normal converter operation. Section II describes the proposed approach for adaptive tuning. Section III presents a numerical design procedure for the MIMO control loop. Experimental results are presented in Section IV using a synchronous buck converter power stage. Conclusions are presented in Section V.

II. ADAPTIVE TUNING CONTROL SYSTEM

A system block diagram for the proposed tuning approach is shown in Fig. 1. The digital controller consists of a voltage A/D converter (ADC), a discrete-time PID compensator, and a digital pulsewidth modulator (DPWM). There are two main components to the adaptive tuning system: a stability margin monitor [14] and a MIMO control loop. The stability margin monitor is a digital implementation of the analog loop gain measurement technique using signal injection, as first described by Middlebrook [15]. The monitor is connected between the output of the PID compensator and the DPWM input. A digital square-wave signal $V_{z}$, with frequency equal to the frequency command $f_{inj}$, is injected in the closed-loop system during normal operation. The magnitude of the injection signal $V_{z}$ is chosen such that only $\pm1$ LSB at the ADC output is triggered, which is the smallest detectable perturbation. Signals $V_{e}$ and $V_{g}$ are...
Fig. 1. Crossover frequency and phase margin monitor and adaptive tuning control loop block diagram. The outputs of the MIMO control loop are the PID compensator zero locations and gain. $G(z)$ is the transfer function from compensator inputs $K$, $Z_1$, and $Z_2$ to stability margin detector outputs.

processed by bandpass filters tuned to $f_{inj}$ to remove unwanted frequency components, and then compared in magnitude using peak detectors. A simple integral feedback controller adjusts the injection frequency $f_{inj}$ so that $\|V_y(f_{inj})\| = \|V_x(f_{inj})\|$. As a result, $f_{inj}$ represents the system crossover frequency $f_c$

$$\|T(f_{inj})\| = \|V_y(f_{inj})\| / \|V_x(f_{inj})\| = 1$$ (1)

Simultaneously, a phase detector measures the phase difference $\varphi$ between $V_y(f_{inj})$ and $V_x(f_{inj})$

$$\varphi = \angle V_y(f_{inj}) - \angle V_x(f_{inj})$$ (2)

to obtain the system phase margin.

The outputs of the stability margin detector, $\varphi_m = \varphi$ and $f_c = f_{inj}$, are compared to the desired reference values $\varphi_{m,\text{ref}}$ and $f_{c,\text{ref}}$, respectively. These error signals are used to adaptively tune the parameters of the compensator $G_c(z)$ in order to achieve the target specifications $f_c = f_{c,\text{ref}}$ and $\varphi_m = \varphi_{m,\text{ref}}$. The proposed approach can be applied to adaptive tuning of various types of compensator structures; however in this paper, a generic PID compensator example is considered with the following transfer function:

$$G_c(z) = K \frac{(z - Z_1)(z - Z_2)}{z(z - 1)}.$$ (3)

As shown in Fig. 1, the adaptive tuning system is driven by the errors between the desired crossover frequency and phase margin and the values measured by the stability margin detector. The error signals, $f_{c,\text{error}}$ and $\varphi_{m,\text{error}}$, are inputs to a matrix of transfer functions used to determine the compensator zero locations, $Z_1$ and $Z_2$, and the gain $K$ such that zero error with respect to the target specifications is achieved. The proposed adaptive tuning system relies on the assumption that the feedback loop behaves as a linear, time-invariant system. This should be taken into account when choosing crossover frequency and phase margin targets for the adaptive tuner.

The matrix $S(z)$ represents the transfer functions from $f_{c,\text{error}}$ and $\varphi_{m,\text{error}}$ to $K$, $Z_1$, and $Z_2$

$$\begin{bmatrix} \dot{K} \\ \dot{Z}_1 \\ \dot{Z}_2 \end{bmatrix} = \begin{bmatrix} A_1 & A_2 & z \\ A_3 & A_4 & z \\ A_5 & A_6 & z \end{bmatrix} \begin{bmatrix} f_{c,\text{error}} \\ \varphi_{m,\text{error}} \end{bmatrix} = S(z) \begin{bmatrix} f_{c,\text{error}} \\ \varphi_{m,\text{error}} \end{bmatrix}.$$ (4)

$A_1$–$A_6$ are designed to achieve stability and desired performance, based on the closed-loop small-signal transfer matrix. To model the closed-loop system, a transfer matrix from inputs $K$, $Z_1$, and $Z_2$ to outputs $f_{inj}$ and $\varphi$ must be determined.
first. In particular, the transfer matrix $G(z)$ of interest can be written as

$$
\begin{bmatrix}
\hat{f}_{inj} \\
\hat{\phi}
\end{bmatrix} =
\begin{bmatrix}
G_{f_{inj} - K} & G_{f_{inj} - z_1} & G_{f_{inj} - z_2} \\
G_{\phi - K} & G_{\phi - z_1} & G_{\phi - z_2}
\end{bmatrix}
\begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2
\end{bmatrix} = G(z)
\begin{bmatrix}
\hat{K} \\
\hat{Z}_1 \\
\hat{Z}_2
\end{bmatrix}.
$$

(5)

Together, (4) and (5) make up a system of loop gains associated with each loop in the MIMO system (6), as shown at the bottom of this page.

In (6), the diagonal elements represent the direct-path loop gains, while the off-diagonal paths represent coupling loop gains (i.e., from $f_c \rightarrow \phi_m$ or $\phi_m \rightarrow f_c$). Based on (6), each loop gain entry can be designed by choosing $A_1 - A_0$, such that the closed-loop transfer matrix is stable and well behaved. The closed-loop transfer matrix can be written, in terms of (6), as

$$
\begin{bmatrix}
\hat{f}_c \\
\hat{\phi}_m
\end{bmatrix} = (I + L(z))^{-1} L(z)
\begin{bmatrix}
\hat{f}_{ref} \\
\hat{\phi}_m_{ref}
\end{bmatrix}.
$$

(7)

Using (7), the stability of the MIMO control loop can be directly determined based on the location of the closed-loop poles [16]. In particular, the closed-loop system described by (7) is exponentially stable if it is proper and has no poles outside the unit circle [16].

### III. Numerical Design of the Adaptive Tuning Control Loop

The experimental testbed, from which the numerical design is performed, is a synchronous buck converter, as shown in Fig. 1, with a digital feedback loop realized using a Xilinx Virtex-IV field-programmable gate array (FPGA). The nominal power stage parameters in Fig. 1 are $L = 4.1 \mu H$, $C = 377 \mu F$, $R = 2 \Omega$, $V_o = 12 V$, $V_{out} = 5 V$, and $f_s = 100 kHz$. The ADC is a TI-TSH1030 sampled once per switching cycle with an effective LSB resolution of 20 mV, or 0.4% of the dc output voltage. The transistors making up the synchronous rectifier in the power stage are IRFR024 N power MOSFETs.

In order to design (7) for desired performance and stability, the indices of (5) must be determined first. In this letter, the modeling is performed based on a design decision to make the stability margin monitor control loop much faster than the adaptive tuning control loop. This allows the dynamics associated with the stability margin monitor loop to be neglected with respect to the adaptive tuning control loop. The waveform illustrating the proposed modeling approach is given in Fig. 2, where as an example the effect of a perturbation in compensator gain is considered. The perturbation occurs at time $(n-1)$ causing the stability margin monitor to update the new monitored crossover frequency very quickly with respect to the next sample of the MIMO control loop $f_c[n]$. The small-signal transfer function from $f_c[n]$ to $\hat{k}[n - 1]$ is then just a one sample delay $t_d$ and a gain scale factor. From a practical point of view, computing analytical expressions for the gain factors require analytically solving for the crossover frequency and phase margin as functions of the compensator coefficients. With a second-order plant model and a second-order compensator (PID), the analytical solution becomes very complicated yielding little intuitive insight. Therefore, in this letter, a numerical computation of the desired gains is performed. Also included in Fig. 2 is a simulation of the dynamics of the monitoring control loop after a perturbation in compensator gain. The simulation, performed in Simulink, shows that it is possible to design the monitoring control loop dynamics to be much faster than those of the adaptive tuning loop so that the aforementioned modeling approach is valid.

In hardware, the sampling rates of both loops are set relative to the injection frequency (crossover frequency) with the stability monitoring loop having considerably faster sampling. By doing so, as the injection frequency changes, the sample rates of each loop will scale in proportion to each other ensuring that the stability monitoring loop is much faster than the adaptive tuning loop despite the injection frequency. In the experimental system, the sampling rate of the stability margin monitor control loop is set to 16 times slower than the injection frequency, while the adaptive tuning loop sampling rate is set 64 times slower than the injection frequency.

Based on the power stage defined before, a nominal PID compensator can be designed for the output voltage feedback loop, using small-signal analysis, to yield slow but guaranteed stable performance. It is assumed that sufficient information about the nominal power stage (i.e., at system startup) is known

$$
L(z) = G(z)S(z) = \begin{bmatrix}
\frac{z (A_1 G_{f_{inj} - K} + A_3 G_{f_{inj} - z_1} + A_5 G_{f_{inj} - z_2})}{z - 1} \\
\frac{z (A_1 G_{\phi - K} + A_3 G_{\phi - z_1} + A_5 G_{\phi - z_2})}{z - 1}
\end{bmatrix}
\begin{bmatrix}
\frac{z (A_2 G_{f_{inj} - K} + A_4 G_{f_{inj} - z_1} + A_6 G_{f_{inj} - z_2})}{z - 1} \\
\frac{z (A_2 G_{\phi - K} + A_4 G_{\phi - z_1} + A_6 G_{\phi - z_2})}{z - 1}
\end{bmatrix}.
$$

(6)
Fig. 3. (a) Lines of constant crossover frequency as functions of compensator gain and zero location. (b) Lines of constant phase margin as functions of compensator gain and zero locations. In (a), the dashed line indicates where the feedback loop changes sign.

such that a conservative compensator design can be performed. Given the experimental system, the following compensator was used for system initialization:

\[ G_c(z) = 1.0 \frac{(z - 0.90) (z - 0.80)}{z (z - 1)} \]  

which yields a system crossover frequency \( f_c = 6.2 \ \text{kHz} \) and phase margin \( \varphi_m = 65^\circ \). Now, using the defined power stage and the compensator given in (8) as the adaptive tuning dc operating point, the small-signal gains given in \( G(z) \) have numerically been computed based on the previously described modeling approach

\[
\left[ \begin{array}{c} \hat{f}_{inj} \\ \hat{\varphi} \end{array} \right] = \left[ \begin{array}{ccc} -4577 & -1138 & 2102 \\ 470 & 1918 & 2239 \\ z & z & z \end{array} \right] \left[ \begin{array}{c} \hat{K} \\ \hat{Z}_1 \\ \hat{Z}_2 \end{array} \right].
\]  

Before designing the indices of (4), a large-signal stability analysis is performed to determine the range over which each loop gain transfer function is monotonic. In particular, because the adaptive tuning system is accounting for power stage parameter changes, the dc operating point around which the MIMO system was designed may significantly change and possibly cause instability. Contour plots of constant crossover frequency and phase margin have been plotted as functions of \( K \) and \( Z_1 \) with \( Z_2 = 0.95 \). These plots can be used to determine the range of tuned compensator parameters over which the indices of (9) do not change sign. Fig. 3(a) and (b) shows that both crossover frequency and phase margin are monotonic for all cases presented except the effect of large zero location changes on crossover frequency. In this case, as the zero location crosses the dotted line indicated in Fig. 3(a), the feedback loop relating \( f_c \) to compensator zero location will change sign, and thus negative feedback cannot be guaranteed about this operating point. This is dealt with in hardware by choosing \( S(z) \) such that any changes in crossover frequency do not directly affect zero locations

\[ A_3 = A_5 = 0. \]  

Although this constraint does limit the control design, it helps widen the range of parameter variations over which the control loops are monotonic.

Similar plots, as given in Fig. 3, can be used to investigate the range of power stage variations over which each feedback loop remains stable. A summary of these results are presented in Table I showing that major variations in all power stage parameters (\( C, L, \) and \( V_g \)) do not cause the feedback loop signs to change. Note that in Table I, each maximum and minimum value

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C )</td>
<td>377 ( \mu )F</td>
<td>1.4 mF</td>
<td>15 ( \mu )F</td>
</tr>
<tr>
<td>( L )</td>
<td>4.1 ( \mu )H</td>
<td>17 ( \mu )H</td>
<td>0.35 ( \mu )H</td>
</tr>
<tr>
<td>( V_g )</td>
<td>12 V</td>
<td>17 V</td>
<td>3 V</td>
</tr>
</tbody>
</table>

Fig. 4. Closed-loop frequency response of the MIMO control system from (a) \( f_c \rightarrow f_c \) ref, (b) \( \varphi_m \rightarrow \varphi_m \) ref, (c) \( f_c \rightarrow \varphi_m \) ref, (d) \( \varphi_m \rightarrow \varphi_m \) ref. Responses (a) and (d) track well up to a given frequency while (b) and (c) reject well, as desired.

Fig. 5. Experimentally observed dynamic performance of the MIMO adaptive tuning control loop. (a) Monitored phase margin in degrees. (b) PID compensator \( z \)-domain zero locations. (c) Monitored crossover frequency in kilohertz. (d) PID compensator gain.
assumes that the other power stage parameters are operating at nominal values.

Beyond the constraint given in (10), the adaptive tuning gains can be designed to achieve desired performance and stability as discussed previously. In the experimental system, the adaptive tuning control loop has been designed to minimize phase margin error faster than the crossover frequency error. This amounts to choosing $A_1, A_2, A_4,$ and $A_6$ such that the closed-loop bandwidth of the direct phase margin loop is greater than the direct crossover frequency path bandwidth. The gains in the experimental system were chosen as follows:

$$\begin{bmatrix} \hat{K} \\ \hat{Z}_1 \\ \hat{Z}_2 \end{bmatrix} = \begin{bmatrix} z (-3.05 \times 10^{-5}) & 0 \\ z - 1 & z (1.11 \times 10^{-4}) & 0 \\ 0 & z (8.38 \times 10^{-5}) & z - 1 \end{bmatrix} \begin{bmatrix} f_{\text{c-error}} \\ \varphi_{\text{m-error}} \end{bmatrix}$$

which leads to a system loop gain matrix of

$$L(z) = \begin{bmatrix} 0.14 & 0.05 \\ (z - 1) & (z - 1) \\ -0.0143 & 0.4 \\ (z - 1) & (z - 1) \end{bmatrix}.$$ (12)

The impact of this design can be discussed based on the closed-loop frequency responses, computed from (7) and (12), and given in Fig. 4. Fig. 4(a) is the closed-loop frequency response from $f_c$ to $f_{\text{c-ref}}$ indicating that crossover frequency reference changes are tracked well up to about 10 Hz, which is the approximate bandwidth of that tuning loop. Similar results are presented in Fig. 4(d) showing that the effect of $\varphi_{\text{m-ref}}$ changes on $\varphi_m$ is tracked up to about 40 Hz. Conversely, Fig. 4(b) is the response of $\varphi_m$ to changes in $f_{\text{c-ref}}$ showing that any changes in $f_{\text{c-ref}}$ do not significantly affect $\varphi_m$ due to the action of the feedback loop. Similarly, Fig. 4(c) indicates that $f_c$ is not significantly affected by $\varphi_{\text{m-ref}}$ changes. Note that the closed-loop bandwidth of the $\varphi_m \rightarrow \varphi_{\text{m-ref}}$ loop is the largest thus ensuring phase margin errors converge fastest. Finally, based on the closed-loop transfer functions, the closed-loop poles can be examined to prove both internal and overall system exponential stability [16]. For the design given by (11), each of the indices of the closed-loop transfer matrix shares the same closed-loop poles given by

$$z_1 = 0.8561$$
$$z_2 = 0.6039$$ (13)

which lie inside the unit circle.

IV. EXPERIMENTAL VERIFICATION

Experimental verification was performed on the same hardware as described in Section III. The adaptive tuning process begins by initializing the system to the nominal compensator
TABLE II
REQUIRED LOGIC RESOURCES TO IMPLEMENT ADAPTIVE TUNING ALGORITHM

<table>
<thead>
<tr>
<th>Function</th>
<th>Logic Gates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Injection/Clock Generator</td>
<td>1762</td>
</tr>
<tr>
<td>Band-pass Filters</td>
<td>2288</td>
</tr>
<tr>
<td>Peak Detectors</td>
<td>1220</td>
</tr>
<tr>
<td>Integral Compensator (Phase Margin Monitor)</td>
<td>1034</td>
</tr>
<tr>
<td>Adaptive Tuning Control Loop</td>
<td>4262</td>
</tr>
<tr>
<td>PID Compensator</td>
<td>1704</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>12270</strong></td>
</tr>
</tbody>
</table>

Given by (8). For this experiment, the target crossover frequency is set at \( f_{c,\text{ref}} = 14.6 \text{ kHz} \), or about one-seventh of the switching frequency, and the target phase margin is \( \phi_{m,\text{ref}} = 40^\circ \). Fig. 5 shows how the compensator parameters adjust to meet target stability specifications from startup, with the compensator given by (8), to steady state when the stability margin references are met. As shown in Fig. 5, after a short time, the compensator parameters have converged and settled to

\[
G_c(z) = \frac{3.63(z - 0.9492)(z - 0.8203)}{z(z - 1)}.
\]  

Based on the discrete-time model of [17], the analytical crossover frequency associated with the compensator given by (15) is \( f_{c,\text{analytical}} = 14.5 \text{ kHz} \) and the analytical phase margin is \( \phi_{m,\text{analytical}} = 39^\circ \), both of which closely match the target values and the values measured by the stability margin monitor.

Fig. 6 is a comparison of load transient performance between the conservatively designed control loop corresponding to the compensator given by (8) and the aforementioned adaptive loop with target crossover frequency \( f_{c,\text{ref}} = 14.6 \text{ kHz} \) and desired phase margin \( \phi_{m,\text{ref}} = 40^\circ \). The conservatively designed control loop exhibits noticeably worse load transient performance after a change in input voltage, while the adaptive loop automatically tunes the controller to maintain desired crossover frequency and phase margin. In Fig. 6(c) and (d), the amplitude of the oscillation due to the signal injection \( V_i \) is about \( \pm 1 \text{ LSB} \) of the voltage sensing ADC, or \( \pm 0.4\% \) of the dc output voltage. Such a small output voltage oscillation caused by the adaptive tuner makes continuous parameter tuning feasible without disturbing steady-state regulation requirements.

As a final note, Table II lists the required logic resources to implement the aforementioned adaptive tuning system and phase margin monitor. Table II indicates that for a reasonable number of gates and no memory requirements, the adaptive tuning controller can be added to any digital system to improve reliability and performance.

V. CONCLUSION

This letter presented a practical method for online adaptive tuning of digital controllers for SMPS. The compensator tuning relies on continuous monitoring of phase margin and crossover frequency, which are outputs of a stability margin monitor. The monitored phase margin and crossover frequency are input to a MIMO control loop that minimizes the error between the desired crossover frequency and phase margin and the measured values. Simple small-signal models are derived and used to design the adaptive tuning control loop to achieve stability over a wide range of operating points. Experimental results presented for a synchronous buck SMPS demonstrated load transient performance, indicating that with the adaptive tuning system, more aggressive and reliable system performance can be achieved as compared to conventional compensator designs. In addition, the hardware requirements for the entire adaptive tuning system are relatively modest making it a practical solution for high-performance power systems.

REFERENCES