Electronic Ballast Control IC With Digital Phase Control and Lamp Current Regulation

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Abstract—A digital control architecture is presented for electronic ballasts that provides a phase sweep for reliable, soft lamp ignition and a smooth transition to lamp current regulation mode. The controller is based on an inner phase loop for fast regulation of the resonant tank operating point and an outer current loop for lamp current regulation. The inner loop operates on a simple digital control law that computes the required gate timing relative to the inductor current zero crossing. Phase control provides reliable drive of the resonant converter in the presence of large dynamic changes in the load impedance during lamp ignition and warm up, natural tracking of component variations with temperature and time. The primarily digital approach provides programmability for broad application, insensitivity to process and temperature variations, realization in low cost CMOS processes and few external components. Experimental results are presented for an integrated ballast controller fabricated in a 0.8 μ CMOS process used in a 400 W, 150 kHz HID electronic ballast.

Index Terms—Current regulation, digital control, electronic ballast, integrated circuit, over voltage protection, phase control.

I. INTRODUCTION

HIGH frequency electronic ballasts are used to provide stable ac drive to a variety of discharge lamps. In many cases, different lamp technologies and applications require unique operating modes and conditions for lamp ignition, normal operation, dimming and protection [1]–[5]. This paper presents a digital control architecture for electronic ballasts that provides a phase sweep for reliable, soft lamp ignition and a smooth transition to lamp current regulation mode. The controller is based on an inner phase loop for fast regulation of the resonant tank operating point and an outer current loop for lamp current regulation, as shown in the simplified diagram of Fig. 1. The inner phase loop operates on a simple digital control law that computes the required gate timing relative to the inductor current zero crossing, resulting in near cycle-by-cycle regulation of the phase of the resonant inductor current \( i_L \) with respect to the square wave drive \( v_{sw} \). Phase control provides reliable drive of the resonant converter in the presence of large dynamic changes in the load impedance during lamp ignition and warm up, natural tracking of component variations with temperature and time, simplified control to output dynamics and a more linear relationship between phase command and lamp current when compared to frequency control [5]–[17].

Application of phase control to electronic ballasts have been shown using analog phase-locked loop (PLL) techniques [7]–[10], self-oscillating circuits [11], [12], and digital PLL [13]. The digital timing techniques in this paper were first presented in [14]–[16], with the benefits of realization in scalable low cost CMOS processes, programmability for broad application, insensitivity to process and temperature variations, and the ability to directly interface with system level digital controllers. A benefit of the system interface is to allow a single core controller to operate independently for lower cost applications (e.g., standard and dimming linear and compact fluorescent lamps, LFL and CFL) that require only basic ignition and current regulation. The same controller may utilize an external system controller for more specialized applications (e.g., high intensity discharge (HID) lamp control with hot re-strike protection and power regulation). The digital interface provides the external controller with sampled information on the ac lamp current and voltage and receives current reference and startup setting commands. The overall architecture was designed for application to a broad range of lamp technologies in order to leverage high volumes for low cost CMOS processing, while limiting the overhead associated with more specialized requirements.

The digital phase control algorithm as applied to the ballast control architecture is presented in Section II, followed by integration of the phase controller with lamp ignition and current regulation blocks in Section III. Experimental results are presented in Section IV for an integrated ballast controller fabricated in a 0.8 μ CMOS process used in a 400 W, 150 kHz HID electronic ballast. Conclusions on the presented work are summarized in Section V. Design details of the analog components in the integrated circuit (IC) controller are given in the Appendix.

II. DIGITAL PHASE CONTROLLER

The direct digital phase control concept, strategy and discrete hardware verification were first presented in [14], [15]. The key concept and control algorithm for realization in the ballast control architecture are given here.

When the LCC resonant inverter of Fig. 1 is operated above resonance, the resonant inductor dominates the resonant tank and thus the inductor current \( i_L \) lags the mid-point voltage \( v_S \) from 0° to 90° as the switching frequency shifts.
Fig. 1. Simplified block diagram of the digital control architecture with two primary ballast control loops: (1) inner phase control and (2) outer lamp current regulation.

Fig. 2. Phase control using inductor current \( i_{L} \) and midpoint voltage \( v_{s} \) in a half-bridge LCC resonant inverter where HS and LS indicate the high side and low side of the half-bridge, respectively.

Fig. 3. State machine for digital phase controller.

The strategy to control the inductor current phase is illustrated in Fig. 2. The essence of the control is to measure the resonant period by detecting the inductor current zero crossing, then compute the required time delays from the zero crossing to determine when to turn on or off the high and low side (HS and LS) gate drives to achieve the desired phase. Given a phase command, the time delay from the zero crossing of the inductor current to the falling edge of the mid-point voltage can be computed as

\[
T_{\text{delay}}[n] = \frac{T_{s}[n - 1]}{4} \left( \frac{(2^m - 1) + (2^m - 1 - \alpha_1[n])}{2^m} \right) - T_{gd}[n - 1]
\]

where \( T_{s} \) is the measured period, \( \alpha_1[n] \) is the digital phase command, \( 0 \leq \alpha_1[n] \leq 2^m - 1 \), \( m \) is the number of bits in the digital phase command. Note that \( \alpha_1[n] = 0 \) corresponds to \( \approx 0^\circ \) while \( \alpha_1[n] = 2^m - 1 \) corresponds to \( \approx 90^\circ \). The final parameter, \( T_{gd}[n - 1] \), is the delay in the gate driver measured in the previous cycle. This optional component is used to compensate phase errors due to gate drive delay [15]. The parameter is measured in each period by counting the time between the edges of the LS command and a feedback signal \( gd_{fb} \) from the actual LS gate (after the driver). Another control approach based on gate drive timing relative to the inductor current waveform is given in [18].

The control algorithm based on Fig. 2 is implemented in the state machine of Fig. 3. Outputs are generated for both the HS and LS gates based on a programmable dead-time. As seen in Fig. 3, phase control is achieved using a single timer to set the gate drive waveforms relative to the inductor current zero crossing. The state machine can be implemented using a microcontroller or directly synthesized in digital logic gates using automated tools, as in the results presented in Section IV.

III. START-UP CONTROLLER AND LAMP CURRENT REGULATION

The purpose of the core outer loop blocks including the start-up controller and compensator block and lamp current peak detector in Fig. 1 is to generate appropriate phase commands \( \varphi \) to perform lamp ignition, warm-up and closed-loop lamp current regulation. Peak detection is performed on the current away from resonance. The output power decreases as the frequency increases above the resonant frequency and the phase angle between mid-point voltage and inductor current increases from \( 0^\circ \) to \( 90^\circ \). Thus the output power can be regulated by controlling the phase angle between the midpoint voltage and the inductor current. The benefits of phase control over frequency control have been described in [5]–[17], as noted in Section I.
lamp current in order to detect lamp ignition and regulate the envelope of the lamp current waveform. Fig. 4 shows a block diagram of the peak detector, which searches for the maximum sampled lamp current \(i_{pk}\) in each switching period. The clock signal \(cycle_{clk}\) is generated by the phase controller.

Fig. 5 shows a block diagram of the combined start-up module and current regulation compensator. The combined block is used to provide smooth transitions between lamp ignition and current regulation. A multiplexer, MUX, is used to select between a phase sweep command \(\varphi_{est}\) and closed-loop current regulation \(\varphi_{cl}\), based on a minimum lamp current threshold \(i_{th}\). The start-up module uses a subtractor and a programmable sweep rate to perform a phase sweep for a controlled progression towards resonance and lamp ignition. Once the peak lamp current exceeds the specified threshold (\(i_{pk} > i_{th}\)), the lamp current compensator takes over. Start phase and minimum phase parameters are also used to protect the ballast, but are not shown in Fig. 5 for simplicity. The integral component of the compensator, \((Z^{-1})\) in the feedback of Fig. 5), is placed on the output of the MUX in order to pre-set the compensator to the phase command \(\varphi\) at the time of lamp ignition. This avoids a sudden step in the command during mode transitions and helps maintain a stable arc in the lamp. Both the peak detector output and compensator delay are latched by the once-per-cycle pulse, \(cycle_{clk}\), from the phase controller.

The compensator is a simple integral only compensator with programmable gain. The design of the compensator is according to the small-signal transfer function \(G_{i_{pk} \varphi}(s)\) from the phase command \(\varphi\) to the sampled peak lamp current \(i_{pk}\). A simulation of \(G_{i_{pk} \varphi}\) is shown in Fig. 6 for the operating parameters shown in the caption. The simulation is generated using the small-signal model developed in [19], neglecting any higher order dynamics of the inner phase control loop. The results show a single pole open-loop response approximated by

\[
G_{i_{pk} \varphi}(s) = \frac{G_o}{1 + \frac{s}{2\pi f_p}}. \tag{2}
\]

Based on (2) a simple integral-type compensator is sufficient to achieve a desired phase margin and high low frequency gain for good lamp current regulation. If the lamp current A/D (analog to digital converter) and effective D/A (digital to analog converter) from the phase controller are interpreted to have unity gain, the loop gain of the outer lamp current regulation loop is given by

\[
T_{\text{lamp}}(s) = -G_{i_{pk} \varphi}(s)G_c(s)H_{\text{lamp}}(s). \tag{3}
\]

where \(G_c(s)\) is the compensator transfer function and \(H_{\text{lamp}}(s)\) is the lamp current sensing gain. The loop gain in (3) includes a negative sign due to the 180° phase shift in \(G_{i_{pk} \varphi}\). This is also why the summation of \(i_{pk}\) in Fig. 5 is positive. The integral-type compensator is given by

\[
G_c(s) = \frac{\beta_{\text{cont}}}{s} \Rightarrow G_c(z) = \frac{\varphi_{cl}(z)}{e(z)} = \frac{\beta}{1 - z^{-1}}. \tag{4}
\]

where \(G_c(z)\) is the discrete-time equivalent of \(G_c(s)\) and \(\beta = T \beta_{\text{cont}}\). The hardware implementation of \(G_c(z)\) in (4) is shown in Fig. 5, where

\[
\varphi_{cl}[k] = \varphi[k - 1] + \beta e[k], \tag{5}
\]

and \(e[k] = i_{pk}[k] - i_{\text{ref}}\) is the error signal. The coefficient \(\beta\) in (5) determined from (2) through (4) by extracting \(G_{i_{pk} \varphi}\) from simulation and solving \(\beta_{\text{cont}}\) to achieve a desired bandwidth or phase margin from (3).
IV. EXPERIMENTAL RESULTS

Experimental results are presented here for a custom IC ballast controller fabricated in a 0.8 μ CMOS process. A more detailed block diagram of the IC controller is shown in Fig. 7. The prototype IC measures 4 mm × 3 mm, including test circuitry and I/O pads. An on-chip oscillator provides 10 ns timing resolution, resulting in 0.18° of resolution in phase regulation at 50 kHz operation and 0.72° of resolution in phase regulation at 200 kHz operation. The phase controller provides the once-per-cycle pulse \( \text{cycle clk} \) based on inductor current positive zero crossing detection to synchronize the peak detector and compensator and also provides a higher frequency synchronized clock \( \text{ADC clk} \) at 32 times the cycle clock frequency for the A/D converter. The phase controller and all logic blocks are synthesized and placed using automated tools.

A digitally controlled oscillator (DCO) block and MUX are used to initiate oscillations in the resonant ballast prior to enabling the phase controller for lamp ignition. If the startup module reaches minimum phase without the lamp current exceeding the threshold, the ballast controller drops back into DCO mode and repeats the ignition sequence. The IC also includes ac buffers for inductor and lamp current and lamp voltage sensing, where ac buffers are used to avoid losses and delays associated with external rectifying circuitry. Lamp voltage sensing is used for over-voltage protection, where the controller will drop back into DCO mode in an over-voltage condition and repeat the ignition sequence. The controller also sends a shutdown signal to the gate driver during an over-voltage condition. Thus high voltage ignitions are avoided and the phase sweep is repeated multiple times until the lamp ignites at a sufficiently low voltage. Details of the analog components of the IC are given in the Appendix.

The controller of Fig. 7 was evaluated on the LCC half-bridge ballast shown in Fig. 8, using a 400 W high output metal halide (MH) high intensity discharge (HID) lamp from GE (MVR400HO). The ballast has a start-up frequency of 170 kHz and full power operation at 135 kHz. The power MOSFETs are
Fig. 9. HID lamp ignition sequence with operating modes labeled, \( V_{dc} = 300 \, V, i_{ref} = 4.8 \, A \).

Fig. 10. Zoom in on HID lamp glow-to-arc dynamics in the first few cycles after ignition.

500 V, 20 A (STW20NM50). A current transformer is used to sense the inductor current \( i_L \), a 0.1 \( \Omega \) sense resistor is used to sense the lamp current \( i_{lamp} \), and a resistor divider is used to sense the lamp voltage \( V_{lamp} \).

Based on the results of Section III and Fig. 6, the compensator gain \( \beta \) is selected as 0.25 to achieve a lamp current regulation loop crossover frequency of approximately 1 kHz. This selection also allows a simple hardware implementation by shifting the bits of the error signal two positions to the left and adding it to the previous phase command. To improve accuracy, the two additional bits are always kept during the internal computation, which gives \( \varphi[k] \) an 11-bit signal. The final output is truncated to give a 9-bit phase command.

Fig. 9 shows a successful lamp ignition sequence with operating modes labeled. Once the lamp ignites, it goes through a short glow-to-arc phase, followed by a warm-up period. During ignition and transition to the warm-up period, the lamp arc is maintained with near cycle-by-cycle regulation of inductor current despite dramatic changes in the lamp impedance. Fig. 10 shows a detail view of the challenging lamp dynamics during the glow-to-arc phase. The lamp current waveform is not sinusoidal due to higher order harmonics associated with lamp ignition, including rectifying behavior prior to stable arc operation. The phase controller is unaffected by these dynamics as it tracks near constant phase despite variations in the tank input impedance. Changes in the frequency of the midpoint voltage are observed as the phase controller maintains an approximately constant phase (due to the small compensator gain used, the phase command is held approximately constant over the several cycles shown). It should be noted that the controller is regulating the peak value of the lamp current in each switching period. As seen during the glow-to-arc operating conditions, the lamp current peaks are not a good representation of the lamp RMS current. A simple improvement to the controller would be to perform a cycle-by-cycle average of the rectified current waveform as a closer approximation to the RMS value with relatively little processing overhead. This would provide higher currents during initial operation and could help to force the lamp out of the glow-to-arc mode more quickly.

Fig. 11 shows steady-state operation of the ballast at a current command, \( i_{ref} = 2.56 \, A \). A Tektronix TDS 3012B 100 Mz oscilloscope with calibrated probes is used to measure the phase between the midpoint voltage \( V_m \) and inductor current \( i_L \). Table I shows the phase and lamp current regulation results over a range of lamp current reference settings, where internal digital values are shown in hexadecimal (H) and scaled decimal values. The first row, DCO, represents fixed frequency operation prior to the phase sweep for ignition. The next four rows represent separate current commands during normal operation. The lamp current measured by the A/D is approximately 90% of the actual current due to a scale factor in the effective anti-aliasing filter at

<table>
<thead>
<tr>
<th>( i_{ref} ) [A]</th>
<th>( P_m ) [W]</th>
<th>( f_s ) [kHz]</th>
<th>( i_{lamp,peak} ) (scope) [A]</th>
<th>( i_{lamp},(digital) ) [A]</th>
<th>( \tau_L ) [A]</th>
<th>Phase ( \phi ) (scope) [deg.]</th>
<th>Phase ( \phi ) (digital) [deg.]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCO</td>
<td>26</td>
<td>167</td>
<td>1.08</td>
<td>06H (-0.96)</td>
<td>2.62</td>
<td>81</td>
<td>FFH (-90)</td>
</tr>
<tr>
<td>1.28</td>
<td>56</td>
<td>152</td>
<td>1.64</td>
<td>09H (-1.44)</td>
<td>3.90</td>
<td>76</td>
<td>FGH (-87)</td>
</tr>
<tr>
<td>2.56</td>
<td>190</td>
<td>141</td>
<td>2.90</td>
<td>10H (-2.56)</td>
<td>7.00</td>
<td>71</td>
<td>DEH (-78)</td>
</tr>
<tr>
<td>3.84</td>
<td>440</td>
<td>135</td>
<td>4.30</td>
<td>17H (-3.84)</td>
<td>10.3</td>
<td>60</td>
<td>CHH (-68)</td>
</tr>
<tr>
<td>4.48</td>
<td>570</td>
<td>134</td>
<td>4.90</td>
<td>1CH (-4.48)</td>
<td>11.7</td>
<td>58</td>
<td>BAH (-65)</td>
</tr>
</tbody>
</table>

Fig. 11. Steady-state operating waveforms for \( i_{ref} = 2.56 \, A \) in Table I. Upper waveform \( V_m \) and lower waveform \( i_L \). The switching period, \( T_s = 7.1 \, \mu s \), \( i_L \) peak-to-peak amplitude and operating phase \( \phi = 71^\circ \) are measured by the oscilloscope.
the input of the IC. The phase regulation has higher accuracy at higher current levels due to the lower switching frequency and corresponding increase in on-chip phase command resolution. The remaining error is due to a delay between the LS gate drive signal and the midpoint voltage, \( v_M \). The error could be removed by sensing \( v_M \) directly, requiring an additional high voltage resistor divider. The absolute phase is only relevant for protection in setting the minimum phase during the ignition sweep and a few degrees of error is allowable.

Finally, Fig. 12 demonstrates over-voltage protection operation with the over-voltage limit set near 3500 V. As shown, the ballast controller repeats the ignition sequence indefinitely until the lamp can ignite below the over-voltage limit.

V. C O N C L U S I O N S

A digital control architecture is presented for electronic ballasts that provides a phase sweep for reliable, soft lamp ignition and a smooth transition to lamp current regulation mode. The controller is based on an inner phase loop for fast regulation of the resonant tank operating point and an outer current loop for lamp current regulation. The inner loop operates on a simple digital control law that computes the required gate timing relative to the inductor current positive zero crossing using a single timer and a simple finite state machine. Phase control provides reliable drive of the resonant converter in the presence of large dynamic changes in the load impedance during lamp ignition and warm up and natural tracking of component variations with temperature and time. The primarily digital approach provides programmability for broad application, insensitivity to process and temperature variations, realization in low cost CMOS processes and few external components. Experimental results are presented for an integrated ballast controller fabricated in a 0.8 \( \mu \) CMOS process used in a 400 W, 150 kHz HID electronic ballast demonstrating reliable operation during all operating modes of the lamp.

FIGURES

Fig. 12. Repeated ignition attempts of HID lamp with over-voltage protection near 3500 V.

Fig. 13. Analog ac buffer block diagram.

Fig. 14. Current mode comparator structure.

APPENDIX

ANALOG INTERFACE BLOCKS

Additional details are given here for the analog interface blocks in the custom IC of Fig. 7, including the ac buffer, A/D and zero-crossing detector circuits. Buffered ac sensing of phase and lamp current and voltage facilitate fast detection, improved efficiency and lower cost by removing external rectifying diodes and filtering. Current-mode circuitry is used for all analog blocks to facilitate ac sensing with minimal external components.

The basic ac buffer structure is shown in Fig. 13, configured for a single-ended input. The buffer provides an output current proportional to the driving voltage with matched external resistors \( R \) [based on two operational transconductance amplifiers (OTAs)]. The OTAs were used instead of operational amplifiers (OPAs) to achieve current-mode outputs and avoid the need for external feedback resistors. The OTAs were implemented using folded cascode techniques with a PMOS input differential pair for an input common mode range that includes the analog ground. The relationship for the output current \( i_{out} \) in Fig. 13 is given by

\[
\frac{i_{out}}{i_{in}} = \frac{v_{in}}{R}.
\]

For inductor current zero-crossing detection, a simple current-mode comparator follows the buffer. This comparator is based on the high speed current-mode approach proposed in [20], with the structure shown in Fig. 14. The output of the comparator is a square wave with a rising edge synchronous to the positive zero crossing of the inductor current waveform. This signal is used by the phase controller to determine the switching period \( T_s \).
For lamp current and voltage A/D conversion, the output current is piped through a channel including an analog current mode rectifier (to simplify A/D), sample and hold, and an asynchronous pipelined A/D converter, as shown in Fig. 15. A conceptual block diagram and description of the current-mode rectifier is shown in Fig. 16. The current-mode comparator and switch are used to steer the input current to the upper mirror for positive values and lower mirror for negative values. A small bias current of $I_B$ is added into the current mirrors to avoid distortion for small input currents, $i_{in}$. The current-mode sample and hold circuit is based on a complete clock-feedthrough (CFT) cancellation approach as described in [21], with a simplified diagram shown in Fig. 17. The sample and hold block samples the full-wave rectified current with a selectable sampling frequency of 16 or 32 times the ballast frequency, based on the synchronized clock $ADC_{clk}$ from the phase controller. This ensures that exactly 16 or 32 samples of output waveforms are taken in each switching period, despite variations in switching frequency.

The 6-bit current-mode A/D is realized using an asynchronous pipelined structure, as shown in Fig. 18 for the first two MSBs (most significant bits). The input current to each stage is compared to 1/2 the reference current $I_{ref}$ to get the digital output for that bit. If the input current is greater than 1/2 the reference current, the bit will be on and 1/2 the reference current is subtracted from the input current. The result is multiplied by two, and then passed to the next stage. If the input current is less than 1/2 the reference current, the bit will be off, and the input current is directly multiplied by two and then passed to the next stage. Two identical copies of the sampling and A/D blocks shown in Fig. 15 are used on the IC for lamp current and voltage sensing.

Experimental results of one complete ac buffer and A/D converter pipeline are shown in Fig. 19 for the lamp current A/D converter clocked at 16 times the ballast frequency. The output is approximately linear and monotonic, but does include a flat band at one half full scale due to mismatch in the binary weighted pipeline cells. The effect of the flat band is to create a nonlinearity in the response. This has minimal effect on the transient behavior through this band since the converter is still monotonic. However, the mismatch error creating the flat band would have to be fixed in order to achieve...
stable lamp current regulation in the flat band region. The experimental results in Section IV with the 400 W HID lamp were performed in the bottom half of the A/D full scale range (below 5 A) in order to avoid the flat band region.

REFERENCES


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