Abstract—In this paper we present a custom IC design and experimental results for a hardware efficient 16 phase digital modulator implemented in a 0.35 µm process. The hardware efficient realization is achieved by time sharing the high resolution portion of the modulator hardware and a simple solution to track phase rotation. The modulator is designed for a duty cycle update rate at 16 times the single phase switching frequency to enable wide bandwidth multiphase converter operation. Two versions of the time shared high resolution portion of the IC are realized, including counter based and self tuning delay line based designs. Design details and experimental results are given to evaluate the two options and demonstrate performance of the IC.

I. INTRODUCTION

A high performance multiphase modulator (MPM) is an essential component in multiphase microprocessor power supplies. A traditional approach to realizing an MPM is to generate a modulation ramp signal for each phase, where the ramp signals are shifted in time to equally space the turn-on of each phase in a single phase switching period. A number of approaches have been proposed and validated recently to emulate traditional MPM operation using digital hardware and a digital input command, with trade-offs between hardware efficiency, versatility and performance [1-4]. Another motivation for use of multiphase converters is to achieve high control loop bandwidth. A digital control approach capable of scaling the bandwidth up with the number of phases was presented in [5], where the output is sampled and duty cycle updated at N times the single phase switching frequency for an N-phase converter. Note that an MPM with a duty cycle update rate of N times the single phase switching frequency is required to achieve the high bandwidth of [5]. A suitable architecture with fast duty cycle update rate and efficient hardware utilization was proposed in [6].

In this paper a custom IC is presented based on the architecture of [6] for a 16-phase MPM with a single phase switching frequency up to 4 MHz and a duty cycle update rate of up to 64 MHz (16 times 4 MHz). A system diagram showing application of the MPM IC in a multiphase buck converter is shown in Fig. 1. Section II describes the MPM architecture and implementation. A description of the custom IC is provided in Section III followed by the experimental results in Section IV.

This work was sponsored by Intel Corporation through the Colorado Power Electronics Center.
MPM approach of [6]. The second is the ability to use the IC in hardware to demonstrate wide bandwidth MPM operation as proposed in [5]. To integrate both functions on to one IC several other logic modules, besides the primary MPM modules, were added. Figure 3 shows the final layout of the IC and Fig. 4 shows a block diagram of the complete IC. Chart 1 gives the dimensions of each of the primary blocks of the MPM. The MPM is made up of two modules: the first is the LSB module which generates the high resolution output; the second is the MSB module which generates the low frequency output and also combines the two outputs. This chip implements two complete version of the MPM on the IC. The only difference between the two designs is the LSB module. In one MPM the LSB module is implemented as a standard counter-comparator DPWM. In the other design the LSB is a delay line that self tunes to the MSB clock. Also included in the chip are two different High Side / Low side (HS LS) drivers and a few MUXs. The HS LS drivers were added so the chip would be compatible with a verity of converters. The MSB and LSB modules are described in more detail in the following subsections. Followed by a discussion on how the two models’ outputs are combined to generate the final gate drive signals. The last subsection will be a description of the 2 HS LS drivers.

A. MSB architecture:

The MSB module is identical for both implementations of the MPM. The purpose of the MSB module is to activate the appropriate number of phases based on the input command and coordinate sequencing (or time shifting) of gate drive signals between the phases. An example of the phased output waveforms is shown Fig. 2.

In hardware the MSB module uses a single counter, called the trailing zero counter, to keep track of which phase just turned off. The value of this counter is then compared with the MSB command to generate the MSB module’s phased outputs. The MSB output has a time resolution equal to the period of the MSB clock signal. The MSB module receives its clock either from the LSB module (for the counter based LSB) or from an external clock (for the self tuning delay line based LSB). The module outputs gate drive signals for each gate at an individual phase switching frequency equal to 1/16th of the MSB clock, up to 4 MHz per phase.

B. LSB architecture

Both versions of the LSB block (the delay line and the counter based) function alike; in other words they generate similar outputs. The counter based LSB uses a signal counter to generate both of its outputs. The delay based LSB uses a delay line to generate its output. Another difference is the delay based LSB uses a 5 bit input instead of the 4 bits the counter version uses.

The counter based LSB uses a high frequency clock signal that is generated off chip. The frequency of the clock is only limited by the hardware, thus any frequency can be used that the hardware can handle. The LSB block uses the high frequency clock to drive its logic and it also divides down this

<table>
<thead>
<tr>
<th>Module</th>
<th>Dimensions [µm]</th>
<th>Area [mm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counter LSB</td>
<td>100x100</td>
<td>0.01</td>
</tr>
<tr>
<td>Delay LSB</td>
<td>443X443</td>
<td>0.196</td>
</tr>
<tr>
<td>MSB</td>
<td>160X160</td>
<td>0.0256</td>
</tr>
</tbody>
</table>

Chart 1: Areas of primary MPM modules

Fig. 2: Timing diagram illustrating how the MSB and LSB outputs are combined to generate the proper phasing and duty cycle for a given input command in a 4-phase system with step changes in the commands. The shaded regions of the Gate Drive output show the LSB output being added to the end of each MSB output.

Fig. 3: The layout of the MPM custom IC
high frequency clock by a factor of 16. The divided, lower frequency clock drives the MSB block. The LSB command is used to determine the duty cycle of the output. The resolution is determined by the number of LSB command bits and in this counter version the resolution is 1/16.

The delay based LSB uses a delay line that locks to the low frequency clock input, the design is based on [7]. Because the delay line was designed to support a certain range of clock frequencies centered around 65 MHz, the clock input must have a frequency around 65 MHz. The LSB output is a square wave with a duty cycle determined by the input command.

C. Gate drive signals

The output of the LSB module is combined with the output of the MSB module to form the final gate driving signals. The combining logic is embedded in the MSB module block. This is convenient because the logic uses the trailing zero counter. As stated above the trailing counter keeps track of which phase just turned off. The phase (also known as the gate drive signal) that is equal to the trailing zero counter is the phase that the LSB output is added. Figure 2 shows that when the trailing zero counter is 1, Gate Drive 1 has the LSB output appended to the end of the MSB output. When the trailing counter equals 2, gate drive 2 has the LSB output, and so on. Only one high-resolution LSB output is needed because no matter how many phases turn off at once only one phase will have the LSB output added to it. This allows application to a large number of phases with relatively little additional hardware. Figure 2 shows the final gate drive waveforms that are generated. The phased MSB output is the non-highlighted portion of the waveform and the LSB output is the highlighted portion of the waveform. The LSB output is added to the gate drive signal that equals the trailing zero count.

D. High Side Low Side Outputs

The MPM chip includes 2 different High side Low side (HS LS) drivers; counter based and delay based. The delay based HS LS driver uses a 4-bit command therefore there are 7 different dead time choices. The delay based HS LS driver is capable of generating a dead time from 0 to 42ns, and with 7 choices the resolution is 6 ns. This is accomplished by using a few simple delay lines to delay the rising and falling edges of the gate drive signal. These delayed edges are used to turn on the HS and LS signals. To turn off the HS and LS signals the non-delayed rising and falling edges, respectively, of the gate drive signals are used.

The counter based HS LS driver is capable of generating dead times from -13.2 ns to +13.2 ns, with a total of 5 options. The driver uses a counter for every phase to generate the dead times. To generate the negative dead time the gate drive signals are delayed by 13.2 ns. This delay gate drive signal is then used to turn on and off the HS and LS signals.

IV. EXPERIMENTAL RESULTS

A test PCB was designed to verify correct operation of the MPM. The test board was designed so that all the chips inputs can be driven by onboard DIP switches or an external source, such as a FPGA. The board also contains both clocks
needed to drive the 2 MPM versions. The delay MPM is
driven by a 64 MHz clock therefore the phase switching
frequency is 4 MHz. The counter MPM is driven by a 150
MHz clock thus a 976 kHz phase switching frequency. An
Agilent 1681AD logic analyzer and a Tektronix TDS7104
oscilloscope were used to capture the chips’ waveforms. The
logic analyzer sampled the waveforms at 800 MHz. The
oscilloscope has a bandwidth of 1 GHz but 500 MHz probes
were used. The experimental results will be presented as
follows: first both the LSB modules and then the MSB
module. Followed by the final gate drive outputs and ending
with the High Side Low Side (HS LS) drivers.

A. LSB modules

Both LSB modules generate a standard PWM output. The
results will be presented in 2 forms. The first will be a figure
showing the LSB output while the LSB command is
increased. The figures will show the pulse width of the LSB
outputs increasing. The second analysis is a D/A
characterization of the LSB output generated by placing a
simple RC filter at the output. The voltage of the waveform
is related to the duty cycle of the LSB output. So as the LSB
command is increased the output voltage of the filter should
increase as well.

1) Counter Based LSB

The counter based LSB module is driven by a 150 MHz
clock. Thus the resolution of the output is 4ns and the MSB
clocks’ frequency is 15.6 MHz. Again the counter based
LSB module has a 4 bit input. Fig. 5 shows the output
increasing as the command increases. The upper waveform
is the MSB clock and the lower waveform is the LSB output.
The input command starts at 0 and increased to 15. It is worth
noting that a command of 15 is not equivalent to a 100% duty
cycle, it is equal to a 93.75% duty cycle. Fig. 6 shows the
D/A characterization of the LSB output. The waveform
ramps up to 3.1 V as expected. The voltage increase of each
step is approximately 1/16th of 3.3 V or 206 mV. Figure 5
and 6 are of the same outputs but just shown in different
ways, Fig.6 is the filtered view of Fig. 5. The pulse width of
the LSB output shown in Fig. 5 can be linearly related to the
voltage steps in Fig. 6.

2) Delay Based LSB

The delay based LSB locks to a 64 MHz clock. The
command input is 5 bit therefore it has a time resolution of
488 ps. The delay line from [7] was slightly modified so that
a PWM output was generated every clock cycle. Unfortunately the output latch was chosen incorrectly and the
LSB output can only generate a proper PWM output up to a
50% duty cycle. This was a design error of the delay line
module and not of the MPM. Even though the output is
incorrect the LSB output waveforms still indicate that the
delay line is functioning and locking to the clock.

Figure 7 shows the delay line output as the LSB command
increased. The LSB output is shown for the command
starting at 0 and ending at 27. The top waveform is the 64
MHz clock and the lower waveform is the delay line LSB
output. One can notice that after the 17th pulse the pulse
width begins to shrink. This effect is because of the error in

the LSB output latch. As stated before the LSB output is only
correct up to a 50% duty cycle after that the pulse width
begins to shrink and eventually ends at a 0% duty cycle. This
is more obvious in the next figure. Figure 8 shows the D/A
characteristic of the LSB output. The voltage steps of the
waveform are proportional to the width of the LSB output pulse. It can be seen that as the LSB command increase from 0 to 17 the voltage, thus the pulse width, increase. At a command of 19 the voltage and the pulse width begin to decrease down to 0. The fact that the steps end up back at zero volts is a good sign that the delay line is locking. The coding error that caused the output decrease has been verified in an FPGA and corrected for future versions.

Again, Figs. 7 and 8 are of the same outputs but just shown in different ways; Fig. 8 is the filtered view of Fig. 7. The pulse width of the LSB output shown in Fig. 7 can be linearly related to the voltage steps in Fig. 8.

B. MSB module

The MSB module is identical for both version of the MPM therefore results from only one MSB module is shown. Figure 9 shows the MSB output as the MSB command increases. This figure shows that the MSB output is properly time shifted and increases with the MSB command. There a transition from 15 to 0 where more then one phase is turned off. This correctly shows all the phases transitioning from the on state to the off state. The next subsection will show more transitioning results.

C. Gate Drive signals

Waveforms of the final gate drive signals are presented in this subsection. The waveforms show that the gate drive signals are properly transitioning. Meaning that during a transition the MSB module is generating the proper phases shifted signals and the LSB output being properly appended to the MSB outputs. This also shows that the LSB outputs are transitioning correctly and that the new LSB output is being appended.

Figure 10 shows the MSB and LSB command stepping up and the delay based gate drive signals responding. At the rising edge of the MSB clock, following the transition of the commands, 9 gate drive signals turn on (gate drive signals 4-12). It is also apparent that the LSB output is being added to the end of the MSB output, shown by M1 and M2. One can also see that the glitch in gate drive 3 is not seen in the oscilloscope waveform.

Figure 11 shows the MSB and LSB command stepping up and
the counter based gate drive signals responding. Again the LSB output is being properly appended to the MSB output. M3 shows that the LSB output is only being added to 1 phase when more then one phase turns off simultaneously.

Fig. 11: The MSB and LSB commands stepping down and the resulting transition of the counter based Gate drive signals. M1 and M2 show that the LSB is properly being appended to the MSB output. M3 shows that the LSB output is only being added to 1 phase when more than one phase turns off simultaneously.

Fig. 12: The D/A characteristic of the counter based MPM. The ramp is linear and monotonic.

Fig. 13: The D/A characteristic of the delay based MPM. The little dips are a result of the error in the delay line LSB. This shows that the LSB, in its exact form, gets appended to the MSB output.

D. High Side Low Side Drivers

Figure 14 shows the counter based HS LS driver outputs. The dead time in this figure is ~13.2 ns. It shows that the HS output turns off 13.2 ns after the gate drive signal rises. The LS turns and the gate drive signal turn on simultaneously. The opposite happens at the falling edge of the gate drive signal. The HS signal and the gate drive signal switch states simultaneously while the LS turns off 13.2 ns latter.

Fig. 14: The counter based HS LS outputs. The dead time is ~13.2 ns. Negative dead time is accomplished by using a counter and delaying the gate drive signal by 13.2 ns.
V. CONCLUSION

A 16 phase digital modulator that is a hardware efficient realization without compromise in hardware or performance was implemented on a 0.35 µm process. The hardware efficient realization is achieved by time sharing the high resolution portion of the design (the LSB output) and using a single counter in the MSB module to track phase rotation. The IC contains two complete multiphase modulators, including a counter-based LSB version and a digital DLL based LSB version. Experimental results demonstrate correct phase operation of the MPM for a 16 phase output and 4 MHz operation per phase.

REFERENCES


