An Online Stability Margin Monitor for Digitally Controlled Switched-Mode Power Supplies

Jeffrey Morroni, Student Member, IEEE, Regan Zane, Senior Member, IEEE, and Dragan Maksimović, Senior Member, IEEE

Abstract—This paper presents a practical injection-based method for continuous monitoring of the crossover frequency and phase margin in digitally controlled switched-mode power supplies (SMPS). The proposed approach is derived from Middlebrook’s loop-gain measurement technique, adapted to a digital controller implementation. A digital square-wave signal is injected into the feedback loop and the injection signal frequency is adjusted while monitoring loop signals to obtain the system crossover frequency and phase margin online, i.e., during normal closed loop SMPS operation. The approach does not require open loop or steady-state SMPS operation and is capable of convergence in the presence of load transients or other disturbances. A method for designing the stability margin monitor, based on small-signal models derived using an envelope modeling approach, is also presented. Experimental results are given for multiple power stage configurations demonstrating close matches between monitored and expected crossover frequencies and phase margins.

Index Terms—DC–DC power conversion, digital control.

I. INTRODUCTION

Switching power converters are nonlinear systems with dynamic responses that depend on the operating point. Typically, switched-mode power supply (SMPS) feedback loops are designed based on linearized small-signal models to achieve desired performance at the nominal operating point. At design time, it is a common practice to measure the system loop gain using a network analyzer to verify the loop stability margins under various conditions. Middlebrook’s injection technique [1] has been a widely adopted approach to measuring loop gain as it does not require breaking the feedback loop. Using this technique, designs can be verified offline to ensure desired performance before system deployment. However, offline performance verification does not provide information regarding the effect of operating changes on system performance after deployment.

With advances in digital control for high-frequency dc–dc converters [2], it becomes possible to consider alternative design and verification techniques leading to improved closed-loop dynamic responses, faster design time, and improved SMPS robustness. In particular, various methods have been proposed to measure converter frequency responses online [3]–[5] or to tune compensator parameters based on an online assessment of the frequency response [6]–[11]. Using these types of approaches, it becomes possible to assess and monitor control loop performance online. In [3] and [4], a pseudo-random binary sequence is injected into the control loop for the purpose of identifying the converter open loop control-to-output ($G_{oc}$) frequency response. During the perturbation process, to obtain accurate information the system should operate in steady state. As a result, these approaches are best suited for one-time frequency response measurement. In [6]–[10], frequency response information is obtained based on purposely induced limit-cycle oscillations, again assuming steady-state operation. Therefore, similar to [3]–[5], these approaches are difficult to apply to continuous system monitoring.

Recently, approaches to monitoring and/or tuning of control loops have been proposed which rely on injection of a digital sine-wave into the control loop [5], [10], [11]. For example, a digital sine-wave can be injected into a digital control loop for the purpose of tuning compensator gain to achieve desired crossover frequency as part of an auto-tuning process [10]. Similarly, in [11], a digital sine-wave is injected into the system and used, in a series of steps, to tune the parameters of a digital compensator for desired crossover frequency and phase margin.

In this paper, inspired by Middlebrook’s analog injection technique [1], a method is proposed to measure the crossover frequency and phase margin in a digitally controlled SMPS online, i.e., during normal closed loop operation. The proposed approach does not require opening the feedback loop and is capable of continuously updating the measured crossover frequency and phase margin in the presence of load transients or other system disturbances. Applications of the technique include fast design time verifications, online dynamic performance monitoring of power supplies in power distribution systems (such as servers or spacecrafts [12]–[14]), and adaptive online tuning of controller parameters [15]. Section II details the proposed approach for monitoring stability margins. Section III presents derivations of small-signal transfer functions for the stability margin monitor from which the system can be designed. Section IV presents experimental results. Conclusions are given in Section V.

II. STABILITY MARGIN MONITOR

Middlebrook’s analog loop gain measurement technique is a well known and widely accepted approach to measuring frequency responses without breaking the feedback loop [1], [16]. Fig. 1 illustrates this approach for the case of voltage injection in series with the loop. The measured gain $T_v(s)$ can be written
Further, when (6) is satisfied, the phase margin can be directly measured as

$$\phi = \phi_m = \angle V_y - \angle V_x. \quad (7)$$

Based on (2)–(7), the crossover frequency and phase margin can be monitored online in digitally controlled systems without requiring any additional power stage information. The monitoring can be performed continuously during normal closed loop operation at the cost of a small output voltage perturbation imparted by the injection source \( V_z \). However, the perturbation amplitude seen at the converter output can be automatically controlled by adjusting the signal injection amplitude \( \delta \), as shown in Fig. 2. Details regarding the design and implementation of each processing block shown in Fig. 2 are presented in Sections II-A–D.

A. Injection Generator and Injection Amplitude Controller

The injection generator creates a 50% duty cycle, square-wave perturbation with frequency adjustable by the frequency command \( f_{inj} \). Practically, this square-wave signal can be generated with a digital counter, running off of a high frequency system clock \( f_{clk} \) and a digital comparator. Since the duty-cycle perturbation is not purely sinusoidal, (2)–(7) no longer hold directly, thus, requiring additional filters as described in Section II-B.

It is of interest to derive the frequency resolution \( q_{f_{inj}} \) of the injection generator as a function of the injection frequency \( f_{inj} \) and the system clock frequency \( f_{clk} \). Begin by defining the ratio

$$n = \frac{f_{clk}}{f_{inj}}. \quad (8)$$

Next, solving (8) for \( f_{inj} \) and then linearizing the equation

$$\frac{\partial f_{inj}}{\partial n} = -\left( \frac{f_{clk}}{n^2} \right). \quad (9)$$

Finally, substituting (8) into (9) yields

$$q_{f_{inj}} = \left| \frac{\partial f_{inj}}{\partial n} \right| = \frac{f_{inj}^2}{f_{clk}}. \quad (10)$$

When the stability margin monitor is operating in steady state, (5) is satisfied and the injection frequency is equal to the crossover frequency. In a typical system, the crossover frequency \( f_s \) is a fraction of the switching frequency \( f_s \), which, in turn is a fraction of the system clock frequency. Hence, high resolution is typically attainable without requiring an unreasonably high-frequency system clock.

To minimize the impact of the signal injection on the output voltage ripple, it is desirable to control the injection signal amplitude \( \delta \) to obtain a minimum detectable output voltage perturbation of \( \pm 1 \) least significant bit (LSB) in the ADC. To ensure minimum output voltage perturbation independent of converter parameters or \( f_{inj} \), the proposed stability margin monitor includes an automatic injection amplitude controller consisting of a feedback loop that adjusts \( \delta \) to achieve the desired perturbation, as shown in Fig. 3. The injection amplitude controller takes as input the quantized output voltage error \( V_{err} \), which is then passed through a peak detector. The peak output voltage error \( V_{err} \) is then...
Fig. 2. Crossover frequency and phase margin monitor block diagram. The outputs of stability margin monitor are crossover frequency and average phase margin of the output voltage loop gain $\Phi$. The injection amplitude controller automatically adjusts the square-wave perturbation amplitude $\delta$ to result in minimum ($\pm1$ LSB) perturbation at the output voltage.

Fig. 3. Block diagram of the injection amplitude controller. The injection amplitude $\delta$ is adjusted via feedback until the desired output voltage perturbation magnitude is achieved compared to the desired LSB perturbation magnitude, $V_{p_{\text{ref}}}$. A simple digital integral compensator adjusts $\delta$ so that the desired output voltage perturbation is achieved independent of $f_{\text{inj}}$.

A secondary benefit to purposely introducing a periodic oscillation into a digital control loop involves improved dc voltage regulation, similar to the approach described in [17]. In particular, the $\pm1$ LSB periodic and symmetric oscillation imposed by $V_z$ at the output voltage combined with the action of the integrator in the PID compensator work to position the dc value of the output voltage in the center of the zero-error bin of the voltage ADC. The accuracy with which the output voltage can be centered in the zero-error bin then becomes a function of the DPWM resolution rather than the ADC resolution.

B. Bandpass Filters and Peak Detectors

As described previously, in the proposed implementation of Fig. 2, $V_z$ is a 50% duty cycle square-wave injection with adjustable frequency determined by the frequency command $f_{\text{inj}}$. However, (2)–(7) are based on the assumption that $V_z$ is a purely sinusoidal injection. To account for the infinite odd harmonics introduced by the square-wave, bandpass filters are used to remove all unwanted frequency components of $V_z$ and $V_y$. The outputs of the bandpass filters, $V_{x_{\text{filt}}}$ and $V_{y_{\text{filt}}}$, then contain only one frequency component equal to the injection frequency.

The bandpass filters, $G_{zp}(z_{bp})$, are designed to be high $Q$-factor filters with the pass-band centered at $f_{\text{inj}}$. However, since $f_{\text{inj}}$ changes in order to continuously satisfy (6), the filter passbands must also change. To realize self-adjustable bandpass digital filters, first consider a general form second-order digital filter

$$G_{zp}(z_{bp}) = A \frac{z_{bp} - 1}{z_{bp}^2 + B z_{bp} + C}. \quad (11)$$

Based on the discrete-time to continuous-time mapping

$$z_{bp} = e^{f_{\text{sample}}} \quad (12)$$

the pass-band center frequency $f_{pb}$ and the $Q$-factor of (11) can be calculated as functions of $B$, $C$, and $f_{\text{sample}}$ (the filter sample frequency)

$$f_{pb} = \frac{f_{\text{sample}}}{2\pi} \left| \tan^{-1} \left( \frac{\sqrt{B^2 - 4C}}{B} \right) \right| \quad (13)$$

$$Q = \frac{1}{2} \left| \frac{\tan^{-1} \left( \frac{\sqrt{B^2 - 4C}}{B} \right)}{\ln \sqrt{C}} \right|. \quad (14)$$
Given $f_{\text{sample}}$, desired $f_{\text{pb}}$ and $Q$, (13) and (14) can be used to solve for the required filter coefficients $B$ and $C$ offline. Coefficient $A$ can then be calculated to achieve the desired filter pass-band gain. After calculating $A$, $B$, and $C$ offline, these coefficients can then be held constant while varying $f_{\text{sample}}$ online in proportion to $f_{\text{inj}}$. In doing so, the filter pass-band center frequency $f_{\text{pb}}$ automatically shifts in proportion to $f_{\text{inj}}$ while $Q$ stays constant (independent of $f_{\text{inj}}$).

Fig. 4 shows sample experimental waveforms, gathered using Chipscope (an embedded FPGA logic analyzer) of the important signals in the stability margin monitor. As shown, the injection source $V_x$ causes a system perturbation seen in both signals $V_x$ and $V_y$. However, since $V_x$ is a square wave causing ±1 LSB output voltage perturbation, $V_x$ and $V_y$ have undesired harmonics as seen in Fig. 4(b). The previously described bandpass filters remove the unwanted frequency components of $V_u$ and $V_x$ such that $V_{y,\text{filt}}$ and $V_{x,\text{filt}}$ contain only the injection source frequency, as shown in Fig. 4(c). In the result shown in Fig. 4, the injection source frequency is approximately equal to crossover frequency because the magnitudes of the filtered signals are approximately equal. Further, the phase margin can be found directly as the phase shift between the two filtered signals.

The digital peak detectors of Fig. 2 take as inputs the filtered waveforms, $V_{y,\text{filt}}$ and $V_{x,\text{filt}}$, and output $V_{y,\text{env}}$ and $V_{x,\text{env}}$, the envelope of the filtered signals. The peak detectors give an assessment of the magnitudes of each signal such that (6) can be continuously satisfied by controlling the injection frequency via a feedback loop.

C. Integral Compensator

An integral compensator with gain $G_i$ is used to process the error between $V_{y,\text{env}}$ and $V_{y,\text{filt}}$, as shown in Fig. 2. Depending on the application and system specifications, a more sophisticated compensator could be used in place of the integral compensator. For the applications considered in this paper however, a very high bandwidth stability margin monitor is not necessary making an integral compensator a sufficient choice. The output of the integral compensator is $f_{\text{inj}}$, the injection frequency command, which is adjusted until there is no error between $V_{y,\text{env}}$ and $V_{y,\text{filt}}$, at which point (6) is satisfied and $f_y = f_{\text{inj}}$.

More detailed design criteria for the integral compensator are presented in Section III.

D. Phase Detector

The phase detector block diagram, used to monitor $\langle \varphi \rangle$, is shown in Fig. 5 and is similar to some approaches used to detect phase in digital phase-locked loops [18]. The phase detector takes as input the filtered signals, $V_{y,\text{filt}}$ and $V_{x,\text{filt}}$. These signals are passed through a digital relay whose output is high when the input is above zero and low when the input is below zero. The two relay outputs are then XOR’d together to form an $\text{Enable}$ pulse, labeled in Fig. 5, which is high whenever the two inputs are not equal. A counter running at the system clock frequency, $f_{\text{clk}}$, measures the length of time $\text{Enable}$ is high which is directly related to the phase shift between $V_{y,\text{filt}}$ and $V_{x,\text{filt}}$.

The main factor in the resolution/accuracy of $\varphi$ is the sample rate, $f_{\text{sample}}$, of the bandpass filters with respect to $f_{\text{inj}}$

$$f_{\text{sample}} = \gamma f_{\text{inj}}$$

where $\gamma$ is an integer proportionality constant. Since $V_{y,\text{filt}}$ and $V_{x,\text{filt}}$ are sampled at a rate proportional to $f_{\text{inj}}$ so that the filter pass-band tracks changes in injection frequency, the respective zero crossings of the two filtered signals could be shifted by as much as one sample period, $1/f_{\text{sample}}$, from the actual zero-crossings. This sampling effect leads to high frequency noise at the counter output $\varphi$ as reported in [19].

To remove the high frequency noise in the measured phase margin, a digital low-pass filter processes $\varphi$, as seen in Fig. 5. The output of the phase detector is then the average value of phase margin, labeled $\langle \varphi \rangle$ in Fig. 5.

III. STABILITY MARGIN MONITOR MODELING

This section aims to derive a model for the digital stability margin monitor from which the integrator $G_i$ can be designed. Before discussing the details of the modeling approach, the experimental test-beds from which the models will be derived are
first introduced. There are two experimental test-beds, shown in Fig. 6, used to verify functionality of the proposed stability margin monitor: a synchronous buck converter and a boost converter which can be operated in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

The nominal power stage parameters of the buck converter are given in Fig. 6(a). The buck converter output voltage ADC is a TI-THS1030 sampled once per switching period with an effective output voltage LSB resolution of 20 mV or 0.4% of the DC output voltage. The nominal switching frequency is 100 kHz.

Nominally, the boost converter power stage parameters are as shown in Fig. 6(b) with \( V_g \) and \( L \) depending on the mode of operation (CCM or DCM). In CCM, \( V_g \text{,CCM} = 15 \) V and \( L \text{,CCM} = 100 \) μH. In DCM, \( V_g \text{,DCM} = 10 \) V and \( L \text{,DCM} = 10 \) μH. The boost converter ADC is an AD7822 with an effective output voltage resolution of 512 mV or 1.6% of the dc output voltage. As with the buck converter, the switching frequency is 100 kHz. A summary of the nominal power stage parameters and the digital compensators used for each test-bed is given in Table I.

The matched bandpass filters used to remove the harmonics of \( V_y \) and \( V_x \) were implemented using the following discrete-time transfer function

\[
G_{bp}(z_{bp}) = 0.00195 \frac{z_{bp} - 1}{z_{bp} - 1.96z_{bp} + 0.998} \quad (16)
\]

where \( f_{sample} = 32 f_{inj} \), i.e., \( \gamma = 32 \) in (15). Choice of \( \gamma \) is generally based on a compromise between the required system clock frequency and the required time resolution of the digital filter. With \( \gamma = 32 \), and assuming a maximum possible crossover frequency of 1/5th \( f_s \), the highest required filter clock frequency is 640 kHz for the experimental prototypes presented here. Based on (13) and (14), the filter pass-band center frequency and \( Q \)-factor can then be calculated as

\[
Q \approx 100 = 40 \text{ dB}. \quad (18)
\]

In order to design the stability margin monitor integral compensator, it is necessary to derive the transfer function from small-signal changes in injection frequency (control) to envelope error (output)

\[
G_{f_{inj} - V_e}(s) = \frac{\hat{V}_{env\_error}(s)}{\hat{f}_{inj}(s)}. \quad (19)
\]

Equation (19) can be determined by first splitting the overall transfer function into two separate transfer functions

\[
G_1(s) = \frac{\hat{V}_{g\_env}}{\hat{f}_{inj}} \quad (20)
\]

and

\[
G_2(s) = \frac{\hat{V}_{z\_env}}{\hat{f}_{inj}} \quad (21)
\]

from which (19) can be found by

\[
G_{f_{inj} - V_e}(s) = G_2(s) - G_1(s). \quad (22)
\]

To compute (20) and (21) and thus determine (22) an envelope modeling approach is used, adapted from resonant inverter modeling techniques [20]–[23]. First, the input perturbation \( V_z \)
This approximation due to the bandpass filters removing all frequency components of \( V_y \) and \( V_x \) except the fundamental component. Next, small-signal variations in \( f_{inj} \) are introduced and represented as a series of signals containing the carrier frequency \( f_{inj} \) and modulated sidebands \( f_{inj} \pm nf_m \) where \( n \) is an integer. Assuming the steady-state injection frequency is much larger than the ac injection frequency variations, all sidebands other than the fundamental can be neglected (i.e., \( n = 1 \)). This approximation allows the small-signal input perturbation to be represented by three distinct frequency components, a carrier signal, \( f_{inj} \), and two dominant sidebands, \( f_{inj} \pm f_m \). This is consistent with the usual narrowband approximations made in resonant converter modeling [20].

With the input decomposed into \( f_{inj} \) and \( f_{inj} \pm f_m \), the response of the system can be determined by the sum of network response to the three distinct input frequencies. More specifically, the system response is determined by the response of the linear transfer functions seen by the input perturbation

\[
H_1(s) = \frac{\hat{V}_{\text{envelope}}}{f_{inj}} = -\frac{T(s)}{1+T(s)} G_{bp}(s) = \frac{N_1(s)}{D_1(s)} \tag{23}
\]

and

\[
H_2(s) = \frac{\hat{V}_{\text{envelope}}}{f_{inj}} = \frac{1}{1+T(s)} G_{bp}(s) = \frac{N_2(s)}{D_2(s)} \tag{24}
\]

Using (23) and (24) and following the approach in [20], it can be shown that the envelope transfer function can be derived as (25), shown at the bottom of this page, where \( n = 1, 2 \).

Using (25), the two envelope transfer functions, \( G_1(s) \) and \( G_2(s) \), can be computed and used to determine the complete envelope transfer function of (22). Finally, computing the stability monitor loop gain as

\[
T_{\text{monitor}} = \left(\frac{\hat{V}_{\text{envelope}}}{f_{inj}}\right) \left(\frac{f_{inj}}{\hat{V}_{\text{envelope}}}ight) = G_{f_{inj}, \text{env}} G_1 \tag{26}
\]

the control loop can be designed by applying standard frequency domain techniques.

The bode plot of \( G_{f_{inj}, \text{env}}(s) \) for the buck SMPS (System 1 of Table I) is shown in Fig. 7(a). As shown in the Fig. 7(a), the envelope transfer function for System 1 consists of a low-frequency real pole, contributed from the poles of the bandpass filters, and a high-frequency real pole present from the closed-loop poles of the output voltage loop.

To verify the accuracy and validity of the envelope model, open loop step responses from the model are compared to an equivalent MATLAB Simulink system simulation. The Simulink simulation consists of the switching power stage along with proposed stability margin monitor running in open loop at a fixed injection frequency. In the simulation, a small step in injection frequency is introduced after which the effect on the envelope error is observed. In Fig. 7(b), the simulated (solid) step response is compared to the step response predicted by the derived model (dashed). As indicated by Fig. 7(b), the predicted step response does not deviate from the simulation result by more than 5%, indicating an accurate modeling approach.

To derive models for the other three experimental systems presented, only \( T(s) \) in (23) and (24) require modification. In particular, each system has a different plant transfer function, \( G_{vd} \) and/or \( G_c \) transfer function and, therefore, \( T(s) \) in (23) and (24) will change for each test-bed. The remaining three experimental systems were modeled with the resulting Bode responses given in Fig. 8. Note that for the analysis presented, the DCM boost converter \( G_{vd} \) transfer function assumes the

\[
G_n(s) = \frac{j V_{inj}}{2s \| H_n(j \omega_{inj}) \|} \left( H_n(-j \omega_{inj}) N_n(s + j \omega_{inj}) D_n(s - j \omega_{inj}) - H_n(j \omega_{inj}) N_n(s - j \omega_{inj}) D_n(s + j \omega_{inj}) \right) \frac{D_n(s + j \omega_{inj}) D_n(s - j \omega_{inj})}{D_n(s + j \omega_{inj}) D_n(s - j \omega_{inj})} \tag{25}
\]
simple, single pole model given in [16]. In all the four models derived in this paper, all high frequency dynamics (above \( \frac{1}{2} f_{inj} \)) are discarded as this system is sampled. It should be noted that the models derived above are in the continuous-time, whereas the stability margin monitor is a digital system operating on discrete-time samples. Therefore, any suitable continuous-time to discrete-time mapping can be used to transform \( G_{f_{inj}, Ve}(s) \) into the discrete domain before designing the digital integrator, \( G_i \).

IV. EXPERIMENTAL RESULTS

The prototypes used to experimentally verify the stability margin monitor operation are the same as summarized in Fig. 6 and Table I. The digital feedback loop was realized using a Virtex-IV FPGA platform with a system clock frequency of 50 MHz. The input injection magnitude \( \delta \) is continuously updated based on the injection amplitude controller until the output voltage error \( V_{err} \) is the minimum possible, \( \pm 1 \) LSB. The speed of the input amplitude controller has been designed to be faster than the monitoring control loop while the sample frequency of the stability margin monitor control loop is equal to the injection frequency. Using the models derived in Section III, four separate control loops were designed for each of the four experimental systems tested. In particular, the control loops were designed, based on the loop gain given by (26), by selecting a \( G_i \) that results in the desired bandwidth with acceptable phase margin. A summary of the gains of the integral gains used to control \( f_{inj} \) is provided in Table II. In addition, Table II also indicates the bandwidth of stability margin control loop relative to its sample rate.

Given the described experimental systems, Table III summarizes the experimental performance of the stability margin

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**TABLE II**

**SUMMARY OF INTEGRAL COMPENSATOR GAINS USED TO CONTROL THE STABILITY MARGIN MONITOR LOOP**

<table>
<thead>
<tr>
<th>System</th>
<th>Integral Gain, G_i</th>
<th>Monitor Bandwidth Relative to Sample Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>System 1 Buck Converter</td>
<td>2.5</td>
<td>0.07%</td>
</tr>
<tr>
<td>System 2 Buck Converter</td>
<td>2.5</td>
<td>0.1%</td>
</tr>
<tr>
<td>System 3 CCM Boost</td>
<td>50</td>
<td>0.04%</td>
</tr>
<tr>
<td>System 4 DCM Boost</td>
<td>7.5</td>
<td>0.05%</td>
</tr>
</tbody>
</table>
monitor with the four different power stage configurations. In Table III, measured output voltage loop stability margins, $f_{\text{inj}}$ and $\langle \phi \rangle$, based on the proposed monitoring approach closely match the values given by the discrete-time model of [24]. Table III also shows measured results based on the standard analog injection technique, obtained by introducing an analog voltage injection at the converter output (Point A in Fig. 5), with the digital stability monitor disabled. The results from the standard analog injection technique indicate close matches with the measurements from the proposed digital technique and the discrete-time model.

Fig. 9 shows the experimentally observed dynamics of $f_{\text{inj}}$, $\langle \phi \rangle$, and $\delta$, captured in Chipscope under an abrupt power stage line transient. In particular, Fig. 9 shows an input voltage change in the synchronous buck converter power stage from 12 to 8 V with the PID compensator of System 1. Under this change, the monitor recognizes the bus voltage change and updates the stability margin monitor outputs accordingly. Note that the high frequency noise seen in the monitored phase margin is an artifact of the bandpass filter sample rate selection discussed previously.

Fig. 10 shows load transient responses for both System 1 (buck converter) and System 4 (DCM boost converter) with the stability margin monitor activated. First, Fig. 10(a) is the load transient response, from 2.5 to 0 A, of System 1 with the phase margin monitor running. Note that the frequency of oscillation imposed by $V_z$ is equal to the crossover frequency while the amplitude of the perturbation is only $\pm 1$ LSB due to the action of the feedback loop controlling $\delta$. Similarly, Fig. 10(b) shows the load transient response for System 4, the DCM boost converter. Since the boost converter is operating in DCM, the load transient (from 0.3 to 50 mA) significantly affects the output voltage loop crossover frequency, as indicated by the oscillation frequency before and after the transient in Fig. 10(b). Note that a comparison of load transient responses with and without the stability margin monitor is given in [19] showing that the proposed system has little effect on the overall dynamic performance of the output voltage control loop.

In the response of Fig. 10, notice the output voltage perturbation combined with the action of the integrator in the PID compensator centers the dc value of the output voltage in the zero-error bin with accuracy related to the DPWM resolution rather than the ADC resolution, as discussed previously. Since in general the DPWM resolution is finer than the ADC resolution, this equates to more precise dc regulation accuracy with the imposed output voltage oscillation.

As a final note, the hardware required to implement the stability margin monitor is summarized in Table IV. As indicated, to implement the entire stability margin monitor requires a relatively modest gate count and no additional memory.

<table>
<thead>
<tr>
<th>System</th>
<th>Buck Converter</th>
<th>CCM Boost Converter</th>
<th>DCM Boost Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Analytical Stability Margins</td>
<td>Digital Stability Margin Detection</td>
<td>Analog Injection Results</td>
</tr>
<tr>
<td></td>
<td>Analytical $f_c$</td>
<td>Analytical $\phi_m$</td>
<td>Measured $f_{\text{inj}}$</td>
</tr>
<tr>
<td>System 1</td>
<td>9.22 kHz</td>
<td>55.0°</td>
<td>9.20 kHz</td>
</tr>
<tr>
<td>System 2</td>
<td>13.8 kHz</td>
<td>27°</td>
<td>13.89 kHz</td>
</tr>
<tr>
<td>System 3</td>
<td>1.20 kHz</td>
<td>85.1°</td>
<td>1.23 kHz</td>
</tr>
<tr>
<td>System 4</td>
<td>6.87 kHz</td>
<td>65.6°</td>
<td>6.42 kHz</td>
</tr>
</tbody>
</table>

Table III

Summary of Experimental Stability Monitoring Results Comparing Stability Margins Based on Model, Measured via Proposed Monitoring Loop and Measured via Traditional Analog Loop Gain Measurement Technique

![Fig. 9](image-url)

Fig. 9. Dynamic response of stability monitor under a change from $V_g = 12$ V to $V_g = 8$ V with the compensator of System 1. (a) Crossover frequency $f_c$, (b) average phase margin $\langle \phi \rangle$, and (c) injection amplitude $\delta$.
Fig. 10. AC coupled output voltage (channel 1) and inductor current (channel 2) waveforms. (a) System 1 (synchronous buck) with crossover frequency and phase margin monitoring during a 2.5 A → 0 A load transient. (b) System 4 (DCM boost) with the crossover frequency and phase margin monitor during a 0.3 A → 0.05 A load transient.

TABLE IV
REQUIRED DIGITAL LOGIC RESOURCES TO IMPLEMENT DIGITAL STABILITY MONITOR

<table>
<thead>
<tr>
<th>Function</th>
<th>Logic Gates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Injection/Check Generator</td>
<td>1262</td>
</tr>
<tr>
<td>Bandpass Filters</td>
<td>2298</td>
</tr>
<tr>
<td>Peak Detectors</td>
<td>1220</td>
</tr>
<tr>
<td>Integral Compensator</td>
<td>1034</td>
</tr>
<tr>
<td>Amplitude Controller</td>
<td>1448</td>
</tr>
<tr>
<td>Phase Margin Monitor</td>
<td>1459</td>
</tr>
<tr>
<td>Total</td>
<td>8711</td>
</tr>
</tbody>
</table>

V. CONCLUSION

This paper has presented a practical method for continuously monitoring the crossover frequency and phase margin in digitally controlled SMPS. The proposed approach does not require open loop operation and is capable of converging to correct results in the presence of load transients or other disturbances. Further, the stability margin monitoring requires and ensures that only ±1 LSB output voltage perturbation is caused by the monitor. Small-signal models are derived by applying an envelope modeling approach and used to design the stability margin monitor control loop. Experimental results are presented using four different system configurations indicating close matches between monitored and expected crossover frequencies and phase margins. Experimental results are also presented showing the observed output voltage and inductor current during a load transient, indicating that the control loop is unaffected by disturbances.

REFERENCES

Jeffrey Mornoni (S’06) received the B.S. and M.S. degrees in electrical engineering from the University of Colorado, Boulder, in 2006 and 2008, respectively. Currently, he is working toward the Ph.D. degree in power electronics from the Department of Electrical and Computer Engineering, Colorado Power Electronics Center, University of Colorado, Boulder.

His current research interests in power electronics include advanced digital control techniques with a general focus on adaptive tuning.

Regan Zane (S’98–M’00–SM’07) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Colorado, Boulder, in 1996, 1998, and 1999, respectively.

From 1999 to 2001, he was with GE Global Research Center, Niskayuna, NY, where he developed custom integrated circuit controllers for power electronic circuits and systems. He has been with the Department of Electrical and Computer Engineering, Colorado Power Electronics Center, University of Colorado, Boulder, since 2001, and as an Assistant Professor from 2001 to 2007, and as an Associate Professor of electrical and computer engineering, since 2008. He has ongoing research programs in energy-efficient lighting systems, adaptive algorithms and digital control techniques in power electronics systems, and low power energy harvesting for wireless devices.

Dr. Zane received the 2004 National Science Foundation CAREER Award, the 2005 IEEE Microwave Best Paper Prize, the 2008 IEEE PELS Transactions Prize Letter Award, and the 2008 IEEE PELS Richard M. Bass Outstanding Young Power Electronics Engineer Award. He received from the University of Colorado the 2006 Inventor of the Year award, the 2006 Provost Faculty Achievement Award, and the 2008 John and Mercedes Peebles Innovation in Teaching Award. He is the Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, LETTERS, and as a Member-at-Large of the IEEE POWER ELECTRONICS SOCIETY (PELS) AdCom.

Dragan Maksimović (M’89–SM’04) received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, Belgrade, Yugoslavia, in 1984 and 1986, respectively, and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1989.

From 1989 to 1992, he was with the University of Belgrade. He has been with the Department of Electrical and Computer Engineering, University of Colorado, Boulder, since 1992, and he is currently a Professor and Director of the Colorado Power Electronics Center there. His current research interests include digital control techniques and mixed-signal integrated circuit design for power electronics.

Dr. Maksimovic received the National Science Foundation CAREER Award in 1997, the Power Electronics Society Transactions Prize Paper Award in 1997, the Bruce Holland Excellence in Teaching Award in 2004, and the University of Colorado Inventor of the Year Award in 2006.