

# Proximate Time-Optimal Digital Control for DC-DC Converters

Vahid Yousefzadeh

Texas Instruments, Digital Power  
v-yousefzadeh@ti.com

Amir Babazadeh, Bhaskar Ramachandran,  
Lucy Pao and Dragan Maksimovic

ECE Department, University of Colorado at Boulder  
{babazade,ramachab,pao,maksimov}@colorado.edu

Eduard Alarcon

Dept. of Electronic Engineering  
Technical University of Catalunya  
ealarcon@eel.upc.edu

**Abstract** - This paper introduces an approach to near time-optimal control in DC-DC converters using a simple digital controller realization. The proposed proximate time-optimal digital (PTOD) controller is a combination of a linear PID controller operating near a reference point and a nonlinear switching surface (NSS) controller away from the reference, together with a smooth transition between the two. A capacitor current estimator enables effective switching surface evaluation and eliminates the need for current sensing. The NSS controller, which is implemented as a small Verilog HDL module, can be easily added to an existing digital PWM controller to construct the PTOD controller. In steady state, the converter operates at constant switching frequency. Simulation and experimental results are shown for a 6.5 V-to-1.3 V, 10 A synchronous buck converter.

## I. INTRODUCTION

In the field of control of switched-mode DC-DC power converters, such as the synchronous buck voltage regulator in Fig. 1, most commonly adopted are standard frequency domain design techniques based on approximate linear time-invariant averaged small-signal models [1]. Starting with the seminal work in [2], it has been recognized that directly taking into account the switching nature of the power stage, and operating with large-signal instantaneous state variables to provide the on-off control action accordingly, can result in improved dynamic responses. The switching surface control [2] and related approaches have afterwards been designated as boundary or geometric control [3].

One case of special interest of the switching surface control results in minimum-time responses, as in the example waveforms shown in Fig. 2(a). By taking into account the converter state trajectories in the two possible switched states,

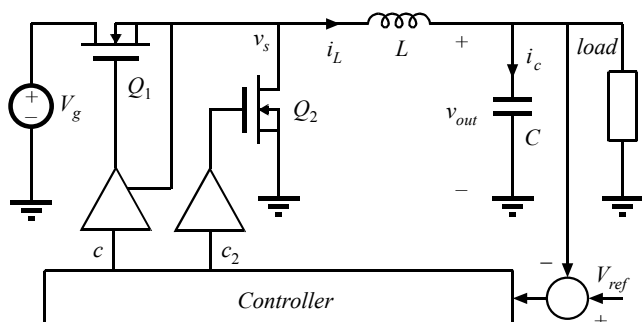
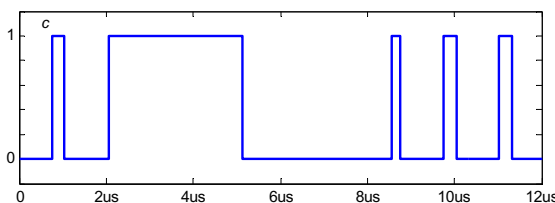
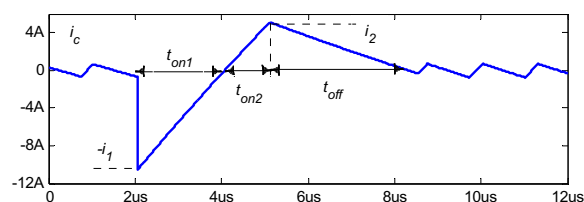
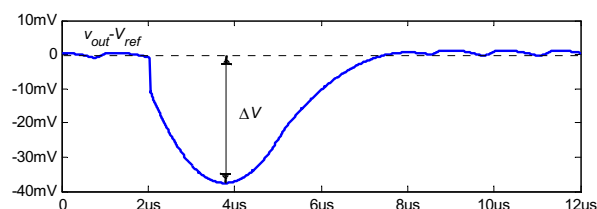
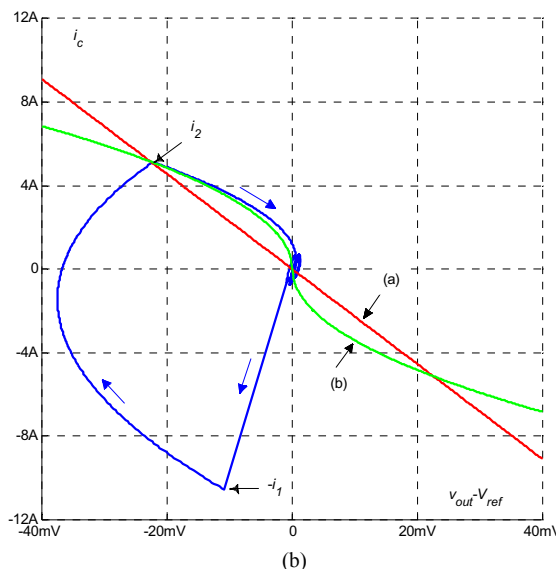


Figure 1: Synchronous buck DC-DC voltage regulator. Prototype example:  $V_g = 6.5$  V,  $L = 1$   $\mu$ H,  $C = 288$   $\mu$ F, switching frequency  $f_s = 780$  KHz,  $V_{ref} = 1.3$  V,  $I_{load} = 0$ -10 A.



(a)



(b)

Figure 2. (a) Waveforms illustrating time-optimal response to a 0-10A step load transient in the converter of Fig. 1. (b) State plane diagram for the 0-10A step load transient, a linear switching surface (a) and a nonlinear switching surface (b).

a switching surface can be derived that naturally provides an on/off sequence that results in the fastest, *i.e.*, time-optimal rejection of large-signal disturbances, as illustrated in the state diagram of Fig. 2(b), which corresponds to the waveforms in Fig. 2(a). Using converter trajectories as switching surfaces for the case of infinite load is discussed in [4], whereas in [5], given the complexity of the theoretical switching surface, the behavior of different approximations is explored. The nonlinear state-feedback that provides time-optimal control can also be derived from an energy transfer approach, as discussed in [6] and more recently in [7]. With the advent of recent applications with more stringent specifications in terms of regulator settling time, various approximations to time-optimal control have recently been proposed, *e.g.*, in [8-10], where time-optimal control is described in terms of boundary control and revisited for the buck converter. Recently, the work discussed in [11] revisits the switching-surface time-optimal control and derives analytically equations for the optimal case, similarly to [4]. Recent works in [12-14] provide a comprehensive account of geometric control principles, including limits of time-optimal control for switching converters.

In the field of general control theory, the fundamentals of time-optimal control, which are directly related to the use of Pontryagin's principle, have been studied extensively [15]. Unfortunately, it has been recognized that ideal time-optimal control may be impractical because of the sensitivity to parameter variations, and unmodeled dynamics [16]. To address this issue, a concept of proximate time-optimal (PTO) control has been proposed [17-20] and successfully applied in, for example, disk-drive head positioning. The main underlying idea considers saturating the control action to facilitate near-time-optimal response to large-signal disturbances and smoothly switching the controller to a standard continuous-time control action in the vicinity of steady state. By combining a time-optimal and a linear controller, it is possible to achieve the favorable properties of both types, namely, fast large-signal transient responses, precise control in steady state, and overall robustness against parameter variations and unmodeled dynamics. The approach presented in this paper is inspired by the PTO ideas and results.

In addition to robustness issues addressed in control theory, a disadvantage that has hitherto precluded widespread use of time-optimal control for DC-DC converters has to do with controller implementation difficulties. In analog controller implementations, the challenges of implementing a nonlinear control law are notable. For example, current-mode circuit techniques to implement squaring functions are proposed in [21], whereas fuzzy approximation techniques are used to synthesize the multi-input nonlinear switching surface in [22].

With advances in digital control for high-frequency switched-mode converters [23, 24], new possibilities arise to consider practical realizations of more advanced control approaches. In particular, Section II briefly reviews previously reported approaches to digital implementation of near time-

optimal or nonlinear control for DC-DC converters [25-31]. Following this review, we argue that proximate time-optimal digital (PTOD) control proposed in this paper, based on a combination of nonlinear switching surface (NSS) and standard linear (*e.g.* PID) control can have advantages in DC-DC voltage regulators where arbitrary load disturbances and realistic component tolerances must be taken into account. An approach to capacitor current estimation, which is a key component of the NSS controller, is introduced in Section III. Section IV describes the complete PTOD controller. Simulation and experimental results for a 6.5V-to-1.3V, 10A synchronous buck point-of-load converter with the PTOD controller are described in Section V. Section VI summarizes the conclusions.

## II. DIGITAL TIME-OPTIMAL CONTROL IMPLEMENTATION APPROACHES

In this section, we use the example in Figs. 1 and 2 to review and discuss approaches to digital realization of near-time optimal control for DC-DC converters.

### A. Programmed On/Off Times

Assuming a specific type of load transient (*e.g.* a step in load), the times  $t_{on1}$ ,  $t_{on2}$  and  $t_{off}$  corresponding to time-optimal response can be found in terms of operating conditions and circuit parameter values using the output capacitor charge balance approach [25-27]. This approach requires implementation of relatively complex computations and also relies on precise real-time inductor current sensing. A combined linear PID and a nonlinear controller with pre-computed on/off times stored in a look-up-table for a limited set of possible step load transients is described in [29]. The approach presented in [30] also combines a linear PID controller with a near-time-optimal controller in transients. Based on detecting the valley (or peak) in the output voltage waveform, the on/off control is executed with the times  $t_{on2}$ ,  $t_{off}$  stored in a look-up table. This approach has advantages of requiring no current sensing, and having relatively simple realization based on continuous-time DSP concept.

### B. Switching Surface

As opposed to computing or programming the on/off times to achieve fast large-signal transient response for a specific type of load transient, a nonlinear switching surface (NSS) controller is based on sensing (or estimating) converter states  $x$ . The switch state, *i.e.*, the switch control signal  $c$  is then determined from

$$c = \begin{cases} 1 & \text{if } \sigma(x) < 0 \\ 0 & \text{if } \sigma(x) > 0 \end{cases} \quad (1)$$

where  $\sigma(x) = 0$  defines the switching surface: the on-to-off switching occurs at the time the converter state trajectory crosses the switching surface. For the case when the states are the capacitor voltage and the capacitor current, Fig. 2(b) shows examples of a linear switching surface and a non-linear switching surface. As discussed in the introductory section, it

has been shown that the switching surface can be designed to enable near-time-optimal responses for the important class of step load transients. Even more importantly, a feedback mechanism is applied at all times, and the controller based on the same switching surface can be shown to result in stable, well-behaved dynamic response in general. This advantage is very significant in DC-DC converter applications where the nature of load transients is generally not known in advance.

The main difficulty associated with implementing (1) in a digital controller is related to sensing or estimation of the converter states. While the output voltage sensing is necessary in any controller realization, it is desirable to consider practical estimation methods to remove the need for precision current sensing. In particular, capacitor current sensing is impractical in most cases. The next section introduces an approach to capacitor current estimation.

### III. CAPACITOR CURRENT ESTIMATION

We consider the case when the output voltage error  $e[n] = V_{ref} - v_{out}[n]$  is sampled by an A/D converter having a least significant bit (LSB) resolution  $q_{A/D}$ , at the rate  $f_{sample} = N_{os}f_s$ , where  $f_s$  is the switching frequency and  $N_{os}$  is the oversampling rate. A very basic finite-difference estimator for the capacitor current is given by

$$i_{cd}[n] = -\frac{C}{T_{sample}}(e[n] - e[n-1]) \quad (2)$$

Fig. 3(b) shows an example of current estimation assuming a very high resolution A/D,  $q_{A/D} = 0$ . Unfortunately, the estimator (2) is highly susceptible to switching noise in the sensed output voltage, and to quantization errors, as illustrated in Fig. 3(c) for  $q_{A/D} = 10$  mV: the effective resolution in  $i_{cd}$  is very low. Low-pass filtering of  $i_{cd}$  can alleviate the problem. For example, applying a moving-average filter of order  $k$  to  $i_{cd}$  in (2) yields a filtered finite-difference estimator:

$$i_{cf}(z) = \left( \frac{1}{k} \sum_{i=0}^{k-1} z^{-i} \right) i_{cd}(z) = -\frac{C}{kT_{sample}}(1 - z^{-k})e(z) \quad (3)$$

which is in digital hardware executed as:

$$i_{cf}[n] = -\frac{C}{kT_{sample}}(e[n] - e[n-k]) \quad (4)$$

One may note that (4) reduces to (2) for  $k=1$ . Fig. 3(d) illustrates the estimation performance of (4). Although an improvement in effective resolution can be observed, a realization of (1) with the capacitor current estimator (4) would still be significantly affected by the quantization errors, especially around zero, and by the delay due to moving-average filtering.

Let us consider an integral estimator of the ac component of the inductor current as an alternative approach. Since  $v_{out} \approx V_{ref}$ , in the buck converter of Fig. 1, the inductor current slopes are  $m_1 \approx (V_g - V_{ref})/L$  and  $m_2 \approx V_{ref}/L$  in the two switch states,  $c=1$  and  $c=0$ , respectively. Since  $i_c = i_L - i_{load}$ , assuming a known initial condition, an integral current estimator can be constructed as:

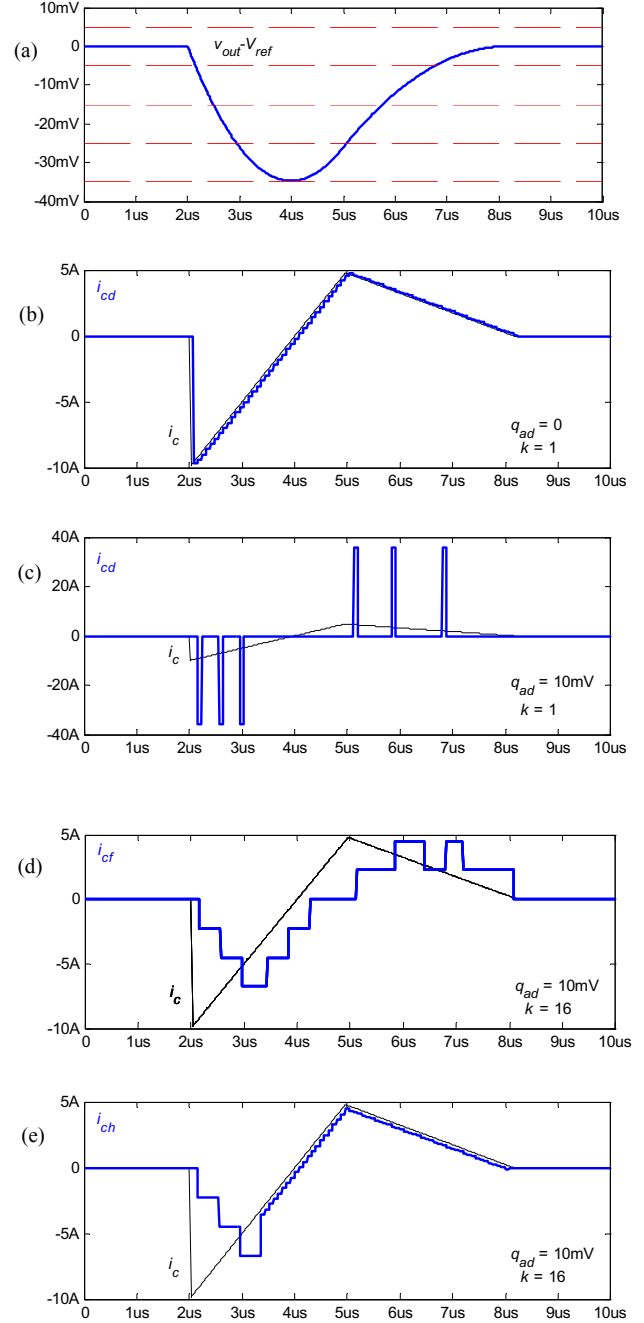


Figure 3 (a) Output voltage waveform during a step-load-transient; (b-e) capacitor current  $i_c$ , and capacitor current estimates  $i_{cd}$ ,  $i_{cf}$ ,  $i_{ch}$ .

$$i_{ci}[n] = i_{ci}[n-1] + \begin{cases} m_1 T_{sample} & \text{if } c = 1 \\ -m_2 T_{sample} & \text{if } c = 0 \end{cases} \quad (5)$$

which is not subject to quantization errors. Unfortunately, this approach is not suitable for detecting fast changes in the capacitor current.

A hybrid estimator  $i_{ch}$ , which is a combination of (4) and (5) is proposed to overcome these difficulties: we start with  $i_{ch}[n] = i_{cf}[n]$ . Then, taking into account the constant delay in

the estimate (4) when following an approximately linear capacitor current ramp, an initial value for the integral estimator (5) is found as:

$$i_{ci} = i_{cf} + \begin{cases} km_1 T_{sample} / 2 & \text{if } c = 1 \\ -km_2 T_{sample} / 2 & \text{if } c = 0 \end{cases} \quad (6)$$

at the point where  $i_{cf}$  in (4) reaches a peak value, e.g., after a fast load transient. From this point on, the integral estimator is employed,  $i_{ch}[n] = i_{ci}[n]$ . To account for arbitrary load disturbances, a reset of the initial value in (5) can be performed based on (6) whenever a large difference between  $i_{cf}$  and  $i_{ch}$  is detected. Fig. 3(e) shows an example of the hybrid estimator performance. Importantly, a high-resolution capacitor current estimate is available around the points where the state trajectory is crossing the switching surface as required in the implementation of the control law (1).

#### IV. PROXIMATE TIME-OPTIMAL DIGITAL CONTROLLER

Fig. 4 shows the complete PTOD controller around a synchronous buck converter. The window-flash A/D has  $q_{A/D}$  LSB resolution and a total of 9 bins around the reference. The constant-frequency PID controller, and the digital pulse-width modulator (DPWM) are the same as in [31, 32]. The PID controller sampling frequency is the same as the converter switching frequency  $f_s$ . The nonlinear switching surface (NSS) controller takes samples of the voltage error  $e$  at the oversampling rate  $N_{os}f_s$ . The NSS controller is realized as a state machine shown in Fig. 5. In the PID state, the NSS controller simply passes the switch control signal from the PID controller to the output,  $c = c_{DPWM}$ . The controller moves to ON1 (or OFF1) transient state when the voltage error and the current estimate  $i_{cf}$  exceed a threshold (equal to one LSB value in the diagram of Fig. 5). In the transient ON/OFF states, the hybrid capacitor current estimator  $i_{ch}$  described in Section

III is employed, and the switching surface is evaluated. For example, a linear switching surface is given by

$$\sigma[n] = -e[n] + \lambda i_{ch}[n] \quad (7)$$

where  $\lambda$  is a slope parameter. The state transition conditions are shown in Fig. 5. It is of interest to note that the NSS controller simply passes on the switch control signal  $c_{DPWM}$  from the PID controller, or enforces  $c = 1$  (in ON states) or  $c = 0$  (in OFF states). The PID controller continues to run at

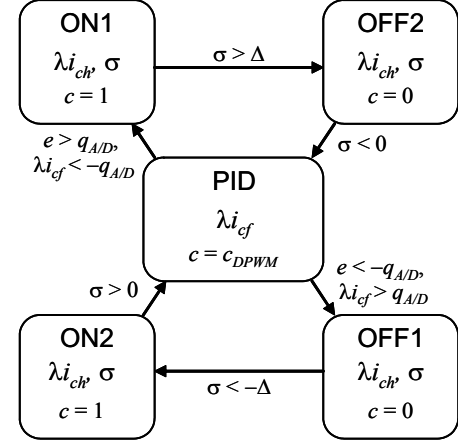


Figure 5 State machine diagram of the NSS controller.

all times, with no modifications required to facilitate smooth transitions. Simulation and experimental results are discussed in the next section.

#### V. SIMULATION AND EXPERIMENTAL RESULTS

Parameters for the experimental synchronous buck converter with the PTOD controller are shown in Fig. 4. The slope parameter in the linear switching surface (7) is such that  $\lambda C / (kT_{sample}) \approx 1$ , so that no multipliers or look-up tables are required in the implementation. The NSS controller state machine (Fig. 5) has been realized in Verilog HDL, resulting in an equivalent gate count of only 386 gates on a Xilinx Virtex IV FPGA development platform. It is worth noting that this very small NSS controller module can be added to an existing digital PWM controller with no other modifications.

In the experimental prototype, the switching frequency is  $f_s = 780$  KHz, and the NSS controller oversampling rate is  $N_{os} = 32$ , which corresponds to the 25 MHz system clock already present in the available PID digital controller realization [31, 32].

Fig. 6 compares performance of the standard PID controller (with the NSS module disabled) against the PTOD controller for three different step-load transients: 75-100%, 50-100% and 25-100%. Significantly improved step-load transient responses can be observed in all three cases.

Fig. 7 shows the experimental waveforms collected by Xilinx Chipscope (an embedded FPGA logic analyzer) for the case of 5-to-10 A step load transient. The normalized switching-surface waveform  $\sigma/q_{A/D}$  indicates the state transitions according to the diagram in Fig. 5.

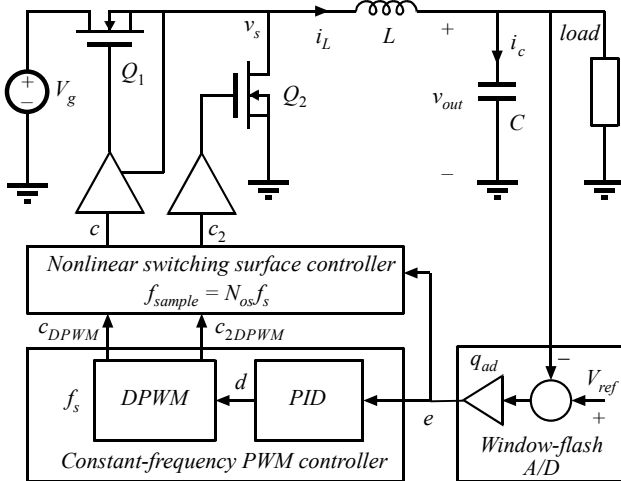


Figure 4 Proximate time-optimal digital controller for a synchronous buck converter. Experimental prototype parameters:  $V_g = 6.5$  V,  $L = 1$   $\mu$ H,  $C = 288$   $\mu$ F (ceramic),  $R_{esr} = 1$  m $\Omega$ ,  $V_{ref} = 1.3$  V,  $f_s = 780$  kHz,  $I_{load} = 0$ -to-10 A,  $q_{A/D} = 10$  mV,  $N_{os} = 32$ ,  $k = 32$ .

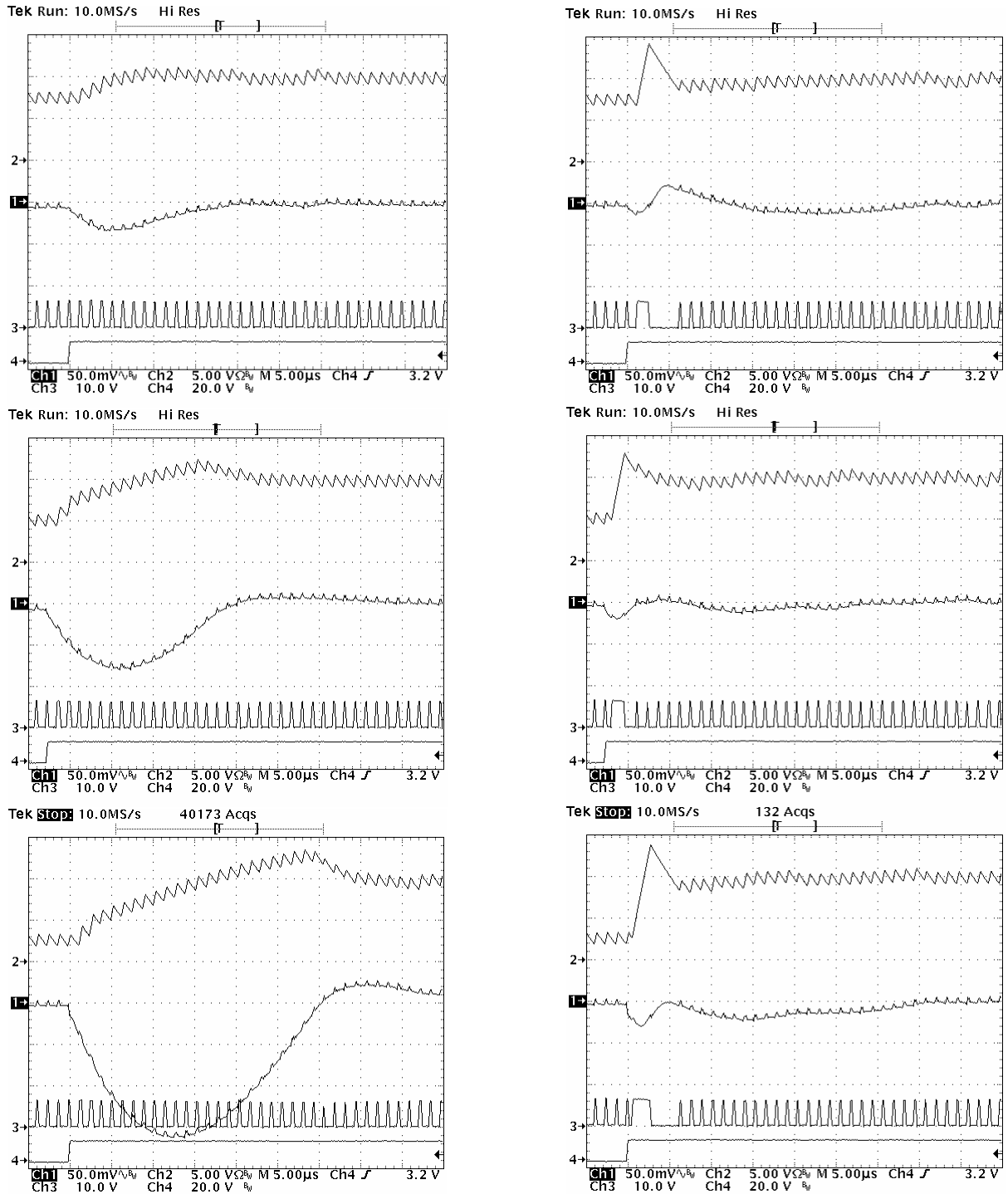


Figure 6: Experimental step-load transient waveforms for the PID controller (left) and the PTOD controller (right). Top: 7.5-10A; middle: 5-10A, bottom: 2.5-10A. The waveforms shown are, top-to-bottom: inductor current  $i_L$  (5A/div), ac coupled output voltage  $v_{out}$  (50 mV/div), switch-node voltage  $v_s$  (10V/div), and load control signal.

The NSS controller enters the ON1 state when the voltage error  $e$  equals  $-2q_{A/D}$ . In the ON1 state, the switch control signal is on,  $c = 1$ , and the switching surface  $\sigma$  is evaluated according to (7). Transition to the OFF2 state occurs at the time  $\sigma$  crosses the threshold  $\Delta = q_{A/D}$ . In the OFF2 state,  $c = 0$ . Finally, upon detection of the zero-crossing of  $\sigma$ , the

controller moves back to the PID state, and the PID controller takes over the task of bringing the output voltage error to the zero-error bin of the A/D converter. Since sensing of the output voltage and evaluation of the switching surface occurs throughout the controller operation, the PTOD controller is capable of providing high performance dynamics under

arbitrary load disturbances. This is in contrast to near time-optimal controllers based on computation or programming of on/off times for a specific type of load transient.

Table I summarizes simulation results investigating robustness of the PTOD controller against parameter variations. The table compares the maximum voltage deviations  $\Delta V$  obtained with the ideal time-optimal controller, the PTOD controller with nominal power-stage parameters ( $L = 1 \mu\text{H}$ ,  $C = 288 \mu\text{F}$ ,  $R_{\text{esr}} = 1 \text{ m}\Omega$ ), the PTOD controller with perturbed power-stage parameters ( $L = 1 \mu\text{H} \pm 20\%$ ,  $C = 288 \mu\text{F} \pm 20\%$ ,  $R_{\text{esr}} = 1\text{-to-}5 \text{ m}\Omega$ ), and the standard PID controller with the nominal parameters. The results show that the PTOD controller consistently results in high-performance responses, even based on the simple linear switching surface (7). Further improvements can be obtained by employing a nonlinear switching surface, by adaptive adjustments of controller parameters, or by on-line parameter tuning (such as [33]), which will be addressed in future work.

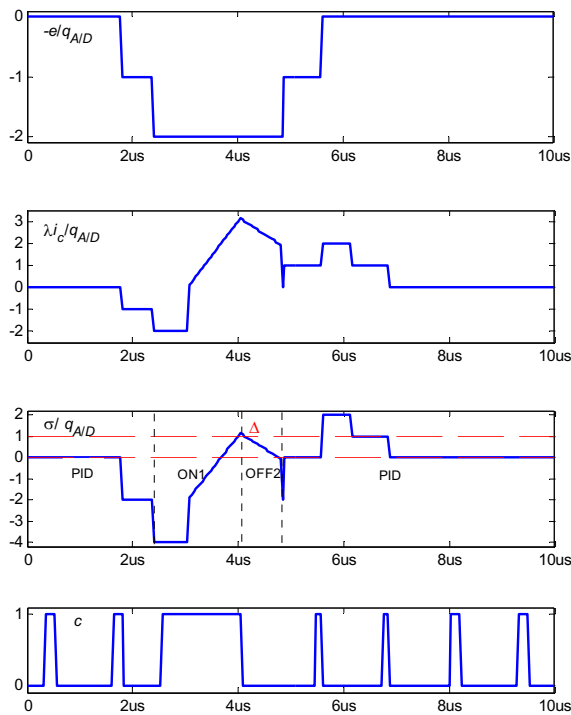


Figure 7 Experimental Chipscope waveforms collected from the FPGA controller prototype for the PTOD controller during a 5-to-10A step load transient.

TABLE I  
PEAK OUTPUT VOLTAGE DEVIATION  $\Delta V$

Step-load transient	Ideal time-optimal	PTOD		PID nominal
		nominal	worst-case	
7.5-10 A	5 mV	27 mV	39 mV	27 mV
5-10 A	12 mV	21 mV	27 mV	54 mV
2.5-10 A	25 mV	30 mV	36 mV	82 mV

## VI. CONCLUSIONS

This paper introduces an approach to near time-optimal control in DC-DC converters using a simple digital controller realization. The proposed proximate time-optimal digital (PTOD) controller is a combination of a linear PID controller operating near a reference point and a nonlinear switching surface (NSS) controller away from the reference, together with a smooth transition between the two modes. A key component of the NSS controller is a hybrid capacitor current estimator that enables effective switching surface evaluation even with a relatively low-resolution hardware, and eliminates the need for current sensing. The NSS controller, which is implemented as a Verilog HDL module, is very small (less than 400 gates). The NSS module can be easily added to an existing digital controller to construct the PTOD controller. In steady state, the converter operates at constant switching frequency. Simulation and experimental results are shown for a 6.5 V-to-1.3 V, 10 A synchronous buck converter.

## ACKNOWLEDGMENT

This work has been sponsored through Colorado Power Electronics Center (CoPEC).

E. Alarcón held a visiting position at CoPEC during summer 2006 with a grant provided by AGAUR, Generalitat de Catalunya. Partial funding by project TEC2004-05608-C02-01 from the Spanish MCYT and EU FEDER funds is acknowledged.

## REFERENCES

- [1] R. W. Erickson, D. Maksimovic, *Fundamentals of Power Electronics*, Springer, 2000.
- [2] W. Burns and T. Wilson, "Analytic derivation and evaluation of a state-trajectory control law for DC-DC converters," in *Proc. IEEE PESC*, 1977, pp. 70-85.
- [3] P. T. Krein, *Elements of Power Electronics*, Oxford University Press, 1998.
- [4] B. Jammes, J. C. Marpinard and L. Martinez-Salamero, "Large-signal control of a buck converter based on time optimal control," in *Proc. ECCTD*, 1993, pp. 1419-1422.
- [5] D. Biel, L. Martinez, J. Tenor, B. James and J. C. Marpinard, "Optimum dynamic performance of a buck converter," in *Proc. ISCAS*, vol. 1, 1996, pp. 589 - 592.
- [6] A. Capel and D. O'Sullivan, "Very high frequency regulator for space applications," in *Proc. IEEE PESC*, vol.1, 1996, pp. 846-852.
- [7] P. Gupta and A. Patra, "Super-stable energy based switching control scheme for DC-DC buck converter circuits," in *Proc. IEEE ISCAS*, vol.4, 2005, pp. 3063-3066.
- [8] K. K. S. Leung and H. S. H. Chung, "Derivation of a second-order switching surface in the boundary control of buck converters," *IEEE Power Electronics Letters*, vol.20, no.2, pp. 63 - 67, June 2004.
- [9] K. S. Leung and H. S. H. Chung, "A comparative study of the boundary control of buck converters using first- and second-order switching surfaces -Part I: Continuous conduction mode," in *Proc. IEEE PESC*, 2005, pp. 2133-2139.
- [10] K. S. Leung and H. S. H. Chung, "A comparative study of the boundary control of buck converters using first- and second-order switching surfaces -Part II: Discontinuous conduction mode," in *Proc. IEEE PESC*, 2005, pp. 2126 - 2132.
- [11] M. Ordóñez, M. T. Iqbal and J. E. Quaicoe, "Selection of a curved switching surface for buck converters," *IEEE Trans. Power Electronics*, vol. 21, no. 4, pp. 1148 - 1153, July 2006.

- [12] J. T. Mossoba and P. T. Krein, "Exploration of deadbeat control for DC-DC converters as hybrid systems," in *Proc. IEEE PESC*, June 2005, pp. 1004 – 1010.
- [13] G. E. Pitel and P. T. Krein, "Trajectory paths for DC-DC converters and limits to performance," in *Proc. IEEE COMPEL*, 2006.
- [14] P. T. Krein, "Feasibility of geometric digital controls and augmentation for ultrafast Dc-Dc converter response," in *Proc. IEEE COMPEL*, 2006, pp. 48-56.
- [15] M. Athans and P. Falb, *Optimal Control: An Introduction to The Theory and Its Applications*, McGraw-Hill, New York, 1966.
- [16] A. S. I. Zinober and A. T. Fuller, "The sensitivity of nominally time-optimal control systems to parameter variation," *Int. J. Contr.*, vol. 17, no. 4, pp. 673-703, 1973.
- [17] W. S. Newman, "Robust near time-optimal control," *IEEE Trans. Automat. Contr.*, vol. 35, no. 7, pp. 841 – 844, July 1990.
- [18] L. Y. Pao, and G. F. Franklin, "Proximate time-optimal control of third-order servomechanisms," *IEEE Trans. Automat. Contr.*, vol. 38, no. 4, April 1993, pp. 560-580.
- [19] L. Y. Pao and G. F. Franklin, "The robustness of a proximate time-optimal controller," *IEEE Trans. Automat. Contr.*, vol. 39, no. 9, pp. 1963-1966, Sept. 1994.
- [20] C. La-orpacharapan and L.Y. Pao, "Shaped time-optimal feedback control for disk-drive systems with back-electromotive force," *IEEE Trans. Magnetics*, vol. 40, no.1, Part 1, pp. 85 – 96, Jan. 2004.
- [21] E. Alarcón, D. Biel, F. Guinjoan, E. Fossas, E. Vidal and A. Poveda, "Current-mode BiCMOS sliding-mode controller circuit for AC signal generation in switching power DC-DC converters," in *Proc. IEEE MWSCAS99*, August 1999.
- [22] S. Gomáriz, E. Alarcón, J. A. Martínez, A. Poveda, J. Madrenas and F. Guinjoan, "Minimum-time control of a buck converter by means of fuzzy logic approximation," in *Proc. IEEE IECON'98*, Aug. 31- Sept 4, 1998, pp. 1060-1065.
- [23] B. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. Power Electronics*, vol. 18, no 1, part 2, pp. 438-446, January 2003.
- [24] D. Maksimovic, R. Zane and R. Erickson, "Impact of digital control in power electronics," *IEEE International Symposium on Power Semiconductor Devices & ICs*, pp. 13-22, May 2004.
- [25] G. Feng, W. Eberle and Y. Liu, "A new digital control algorithm to achieve optimal dynamic performance in DC-to-DC converters," in *Proc. IEEE PESC*, June 2005, pp. 2744 – 2749.
- [26] G. Feng, E. Meyer and Y. F. Liu, "High performance digital control algorithms for DC-DC converters based on the principle of capacitor charge balance," in *Proc. IEEE PESC*, June 2006.
- [27] E. Meyer, G. Feng and Y. F. Liu, "Novel digital controller improves dynamic response and simplifies design process of voltage regulator module," in *Proc. IEEE APEC 2007*, pp. 1447-1453.
- [28] J. Quintero, A. Barrado, M. Sanz, A. Lazaro and E. Olias, "Experimental validation of the advantages provided by linear-non-linear control in multi-phase VRM," in *Proc. IEEE APEC 2007*, pp. 707-713.
- [29] A. Soto, P. Alou, J.A. Cobos, "Nonlinear digital control breaks bandwidth limitations," in *Proc. IEEE Applied APEC*, 2006.
- [30] Z. Zhao, V. Smolyakov and A. Prodic, "Continuous-time digital signal processing based controller for high-frequency DC-DC converters," in *Proc. IEEE APEC 2007*, pp. 882-886.
- [31] H. Hu, V. Yousefzadeh and D. Maksimovic, "Nonlinear control for improved dynamic response of digitally-controlled DC-DC converters," in *Proc. IEEE PESC*, June 2006.
- [32] V. Yousefzadeh, T. Takayama and D. Maksimović, "Hybrid DPWM with digital delay-locked loop," in *Proc. IEEE COMPEL*, June 2006.
- [33] M. Shirazi, L. Corradini, R. Zane, P. Mattavelli and D. Maksimović, "Autotuning techniques for digitally controlled point-of-load converters with wide range of capacitive loads," in *Proc. IEEE APEC 2007*.