Abstract—An architecture is presented for digital multiphase modulators (MPM) that leads to an efficient, high performance hardware realization. The combined modulator, switching phases and output filter are viewed as a multilevel digital-to-analog converter with high power output, or a power D/A, and concepts used in D/A converters are leveraged to achieve high performance and hardware efficiency. The modulator is split into three functional blocks including a decoder that determines how many phases are on at any time, a selector that determines which phases are on at any time, and a single high-resolution module that is time-shared among all phases. The resulting architecture scales favorably with a large number of phases and facilitates fast update rates of the input command well above the single phase-switching frequency, \( f_s \). Experimental results are presented for a custom integrated circuit realization in a 0.35-\( \mu \)CMOS process, designed for 16-phase output with an input command update rate of 16 times \( f_s \). Two complete 16 phase MPM designs are verified on the IC with different high-resolution modules, including a delay-line based design achieving 9-b resolution at \( f_s = 4 \) MHz and a counter-based design achieving 8-b resolution at \( f_s = 586 \) kHz.

Index Terms—Converter, digital, electronics, integrated circuit (IC), modulator, multiphase, power, pulsewidth modulation (PWM).

I. INTRODUCTION

Fig. 1 shows a multiphase dc–dc converter with \( N \) synchronous buck converters (or phases) operating in parallel to achieve improved power scaling, ripple and dynamic performance. Increasing the number of phases, \( N \), is motivated by the potential for scalable monolithic integration [1] and the possibility for closed-loop bandwidth to exceed the switching frequency limits [2], [3]. In this letter we focus on architecture and realization of a high-performance digital multiphase modulator (MPM) to support multiphase systems with a large number of phases \( N \).

A number of previous approaches to realizing digital multiphase modulators [4]–[8] require area intensive dedicated timing generation hardware for each phase in order to generate output signals that are time shifted by \( T_s/N \), where \( f_s = 1/T_s \) is the per-phase switching frequency. An \( N \)-phase system requires \( N \) high-resolution digital pulse-width modulators, which limits the scalability of these approaches. A different architecture, requiring a single high-resolution unit for an arbitrary number of phases has been described in [9], [10]. This approach is based on the assumption that all phases operate with exactly the same duty cycle over each switching period \( T_s \), and that the pattern of switching transitions for individual phases can be determined based on the duty-cycle command once per switching period \( T_s \). This architecture leads to a very efficient, scalable hardware realization but limits the update rate to the switching frequency, \( f_s \).

The MPM architecture and the realization described in this paper are based on the multiphase converter viewed as a multi-level digital-to-analog converter, or power D/A [2], [3], [11], [12], similar to concepts known in digital audio applications [13]. As shown in Fig. 1, a \( p \)-bit digital command, \( d \), is the input to the MPM, which determines how many and which phases are on \( (c_i = 1) \) or off \( (c_i = 0) \) at any given time in order to adjust the analog output voltage, \( v_o \). The proposed MPM architecture, which is introduced in Section II, includes a single high-resolution module. In addition, the MPM input command, \( d \), can be updated at any time, which opens the possibilities for wide-bandwidth closed-loop operation. Experimental results for a custom 0.35-\( \mu \)CMOS integrated circuit with two versions of
a 16-phase MPM are presented in Section III. Section IV concludes the paper.

II. MULTIPHASE MODULATOR ARCHITECTURE

When using two-state switching converters, such as the synchronous buck converter phases shown in Fig. 1, each phase has a single logic high or low control signal, \( c_i \in \{0, 1\} \), that determines the state of the switches in that phase. The purpose of a digital multiphase modulator is to generate the on/off control signals \( \{c_0, c_1, \ldots, c_{N-1}\} \) for each of the \( N \) gate drives in the multiphase converter system based on the high-resolution (\( p \)-bit) input command \( d \).

A general block diagram of the proposed MPM architecture is shown in Fig. 2. The high-resolution \( p \)-bit command, \( d \), is split into an \( n \)-bit MSB (most-significant-bit) portion, \( d_{\text{MSB}} \), and an \( m \)-bit LSB (least-significant-bit) portion, \( d_{\text{LSB}}, p = n + m \). In this letter, \( N \) designates the number of phases in the system and \( n \) designates number of MSBs in the command \( d \). The MSB command, \( d_{\text{MSB}} \), is the input to the MPM core consisting of a Decoder and a Selector. Based on the input, \( d_{\text{LSB}} \), the Decoder sets the signals, \( t_i \), to decide how many phases are on. For example, to turn \( k \) phases on, we have:

\[
t_i = \begin{cases} 
1, & 1 \leq i \leq k \\
0, & k + 1 \leq i \leq N - 1
\end{cases} \quad (1)
\]

The Selector decides which \( k \) phases are on by mapping the signals \( t_i \) to the phase on/off control signals \( c_i \). Finally, a single LSB module complements the MPM core to achieve high-resolution control based on the \( m \)-bit LSB input \( d_{\text{LSB}} \). The architecture in Fig. 2 is very general. The fact that it resembles a standard D/A converter architecture lends immediately to a number of implementation options. For example, if all \( N \) phases are nominally identical (as in Fig. 1), the Decoder converts the binary input \( d_{\text{LSB}} \) to a thermometer-code output \( \{t_i\} \). If, instead, the phases are logarithmic (as in [14]), no decoding is necessary. If the command \( d \) is used to enable and disable \( N \) converter cells and the individual power converters have high-impedance outputs, as is the case with converters having an inner current control loop [14], or with resonant converters [15], the Selector function is trivial, \( c_i = t_i \). In contrast, in the standard multiphase converter of Fig. 1, the Selector has to perform a time-dependent mapping from \( \{t_i\} \) to \( \{c_i\} \) to accomplish, for example, the benefits of ripple minimization and equal current sharing. The LSB module generates a single high resolution timing signal \( t_0 \) that provides fine increments to the on time of the appropriate phase as determined by the Selector. Many options are available for realizing the single high-resolution LSB module, including auxiliary analog regulators [14], [15], or various digital pulse-width modulation (DPWM) techniques [16]–[20]. Finally, we note that the MPM architecture of Fig. 2 allows applications of further resolution-enhancement techniques such as dithering [21] or \( \Sigma \Delta \) modulation [22]–[24].

We focus now on a simple hardware-efficient MPM realization for the multiphase converter in Fig. 1. The solution presented in this letter is based on the following assumptions: all \( N \) phases are nominally identical with the same steady-state command \( d \), and the number of phases is a power of 2, \( N = 2^n \). The number of bits required in the LSB portion is given by \( m = p - n \). For this case, a simple hardware realization according to the MPM architecture of Fig. 2 is shown in Fig. 3. More general solutions to the architecture of Fig. 2 are possible, but require more complex decoder and selector hardware. The binary-to-thermometer decoder sets signals \( t_i \) to turn on \( k \) phases according to command \( d_{\text{LSB}} \). The static characteristic

\[
V_o = \frac{k}{N}V_g = \left( \frac{1}{N} \sum_{i=1}^{N-1} t_i \right) V_g = d_{\text{LSB}} V_g \quad (2)
\]

resembles the characteristic of a standard \( N \)-level thermometer code D/A converter. It is important to note that (2) implies that the same output voltage level is generated regardless of which \( k \) phases are on. This is decided by the Selector, which performs a time-dependent mapping from \( \{t_i\} \) to \( \{c_i\} \). In the realization of Fig. 3, the mapping is done in a rotating manner that results in standard phase-shifted PWM outputs, \( \{c_i\} \), as illustrated by the waveforms in Fig. 4 for the case of \( N = 4 \) phases,
Fig. 4. Timing diagram of the digital MPM architecture for a four-phase system with a step changes in the input command, \( n = 2, m = 3 \).

A single \( n \)-bit down-counter (e.g., counts in reverse \( \{2, 1, 0, 3, \ldots\} \)) and \( N \) multiplexors are used to achieve phase rotation. The LSB command, \( d_{\text{LSB}} \), is input to a single DPWM to generate the PWM signal \( t_0 \). Hardware efficiency is achieved by time-sharing the single high-resolution DPWM output, \( t_0 \), among all \( N \) phases. The Selector naturally appends the high resolution \( t_0 \) component to the falling edge of the on/off control signal, \( c_i \), designated by the phase rotation counter. Phase rotation and the DPWM operate at a clock rate of \( N f_s \), where \( f_s = 1/T_s \) is the single phase-switching frequency. Similar solutions have been used in audio signal-processing D/A converters to achieve high resolution and improved linearity by using phase shifting to allot equal time to each element in the D/A [13].

It is important to note that the MSB input command \( d_{\text{MSB}} \) passes through the Decoder and the Selector directly to generate the on/off control signals \( c_i \). This allows the input \( d \) to be updated at any time, for example at the rate of \( N f_s \) as shown in Fig. 4. For the \( d_{\text{MSB}} \) command transition from 3/4 to 1/4, the number of on phases switches from 3 to 1 instantaneously. The fast update rate and the ability to change the number of phases that are on at any time opens the possibilities for wide-bandwidth closed-loop operation [2], [3].

### III. EXPERIMENTAL RESULTS

A custom integrated circuit (IC) was developed and tested based on the architecture shown in Fig. 3 for a 16-phase output, \( n = 4, N = 16 \). The IC was fabricated in a 0.35 \( \mu \)CMOS process and includes two complete versions of the digital MPM, as shown in Fig. 5. Both versions include identical copies of the MPM core but with different types of DPWM LSB modules: counter and delay-line based. The area requirements for each of the modules and total MPM designs are shown in Table I.

The delay-line based MPM was designed for a clock signal frequency, \( f_{\text{clock}} = N f_s = 64 \text{ MHz} \), resulting in a single phase-switching frequency, \( f_s = 4 \text{ MHz} \). The delay-line LSB was designed using a digital delay-locked loop (DLL) to self-tune to the clock input with a 2:1 tuning range, as introduced in

![Fig. 5. CAD image of the digital multiphase modulator IC realized in a 0.35 \( \mu \)CMOS process depicting two complete MPM designs: (1) with a counter based LSB module and (2) with a delay-line based LSB. Markers indicate location of the MPM core and corresponding LSB module for each design.](image-url)

### TABLE I

<table>
<thead>
<tr>
<th>Module</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counter-based MPM</td>
<td>0.04 mm²</td>
</tr>
<tr>
<td>MPM Core</td>
<td>0.03 mm²</td>
</tr>
<tr>
<td>Counter LSB</td>
<td>0.01 mm²</td>
</tr>
<tr>
<td>Delay-line based MPM</td>
<td>0.23 mm²</td>
</tr>
<tr>
<td>MPM Core</td>
<td>0.03 mm²</td>
</tr>
<tr>
<td>Delay-line LSB</td>
<td>0.20 mm²</td>
</tr>
</tbody>
</table>
[19]. The timing resolution is 488 ps, resulting in a \( d_{\text{LSB}} \) resolution of \( m = 5 \) and overall MPM input command resolution of \( p = 9 \).

The counter-based MPM was designed for a clock signal frequency, \( f_{\text{clock}} = 9.4 \) MHz, resulting in a single phase-switching frequency, \( f_s = 586 \) kHz. The LSB module uses an internal high-frequency clock of \( 16 \cdot f_{\text{clock}} = 150 \) MHz to achieve a timing resolution of 6.6 ns, resulting in a \( d_{\text{LSB}} \) resolution of \( m = 4 \) and overall MPM input command resolution of \( p = 8 \).

Experimental results for the digital MPM are shown in Figs. 6 and 7. All results were captured using an Agilent 1681AD logic analyzer to capture all sixteen phase outputs and a Tektronix TDS7104 oscilloscope, triggered from the logic analyzer to correlate the waveforms. Fig. 6 shows the outputs of the delay-line based MPM as the input \( d \) is sequenced through all possible values of \( d_{\text{NSB}} \) with \( d_{\text{LSB}} = 0 \). Note that all outputs turn off immediately when the input steps from \( d = 15 \) to \( d = 0 \). Fig. 7 shows the outputs of the counter-based MPM around a step change in both the \( d_{\text{NSB}} \) and \( d_{\text{LSB}} \) components of the input \( d \). Again, note the direct feed-through of the \( d_{\text{LSB}} \) command to the outputs at the fast update rate, \( f_{\text{clock}} = N \cdot f_s \).

IV. CONCLUSION

A digital multiphase modulator has been presented that leads to an efficient, high performance hardware realization. The modulator and converter system is viewed as a multilevel power D/A to achieve improved performance and hardware efficiency. The modulator is split into three functional blocks including a decoder that determines how many phases are on at any time, a selector that determines which phases are on at any time and a single LSB module that is time-shared among all phases to achieve high resolution in steady state. The resulting architecture scales favorably with a large number of phases, facilitates fast update rates of the input command well above the single phase-switching frequency and is compatible with a wide range of known DPWM techniques for the LSB module and resolution-enhancement techniques such as dithering or \( \Sigma \Delta \) modulation. Experimental results are presented for a custom IC realization in a 0.35 \( \mu \)CMOS process, designed for 16 phase output with an input command update rate of 16 times \( f_s \). Two complete 16-phase MPM designs were verified on the IC with different high-resolution modules, including
a delay-line based design achieving 9-b PWM resolution at $f_s = 4$ MHz and a counter-based design achieving 8-b PWM resolution at $f_s = 586$ kHz.

REFERENCES


