Abstract – This paper introduces a modular power converter architecture based on series input connected converter cells with independent outputs that each drive a small series string of LEDs. The approach provides the benefits of operating from a high bus voltage while using low voltage cells that independently regulate LED currents for improved light uniformity and LED failure mitigation. Stability of the series converter string and independent regulation of the floating LED output currents are achieved using a two-loop controller that relies on chain control communications between cells to share system information. Experimental verification of input bus voltage sharing and independent cell current regulation is provided using a prototype of the proposed system with four series buck-boost converter cells, where each cell drives four 700 mA LEDs.

Keywords – solid-state lighting, light emitting diodes, LED, digital control, modular systems, series input, power converter

I. INTRODUCTION

Significant improvements have been achieved over the past decade in solid state light emitting diodes (LEDs), leading to high efficiency and high brightness solutions that are expected to surpass and replace existing lighting systems in many applications over the coming decade [1,2]. Although the trend is towards development of higher current and brightness LEDs, practical solutions for replacing large lighting panels in general lighting applications still require use of many LEDs in a system [3]. Typical solutions place many if not all of the LEDs in a series string when operating from a high voltage supply such as the rectified ac line. In addition, current limiting and regulation of each LED string is required to achieve the specified luminous output and light uniformity in the presence of variations in the LED forward voltages [4] and applied input voltage. Existing solutions for current regulation in LED strings include use of series resistors or linear regulators [5] or a single high voltage switching converter [6] per string. Each of these solutions has drawbacks, including low efficiency for series linear elements and high component stress and cost for high voltage converters. Existing solutions also have limited flexibility, requiring all LEDs in a large series string to operate at the same current. The limitations make it difficult to compensate for variations in light output among LEDs and individual LED failures in the system.

This paper introduces a modular architecture, as shown in Fig. 1, based on series input connected power converter cells with independent outputs that each drive a reduced number of series LEDs. The converter cells share the same input current but self-adjust their respective input voltages to properly share the total input bus voltage. The result is a modular architecture that can operate from a high bus voltage using low voltage converter cells. The approach has the flexibility to independently regulate the currents in smaller sub-strings of LEDs for improved light uniformity and LED failure mitigation.

II. SYSTEM DESCRIPTION

A. System Analysis

A block diagram of the system structure is shown in Fig. 1, with detail given for one series string of converter cells. The number of converter cells in a string is based on the voltage rating for each cell. The total number of LEDs associated with a string (sum of LEDs at output of each cell) depends on the size of the system, but is preferably selected to maximize efficiency by setting the nominal converter conversion ratios to near unity. The approach can be extended to larger systems by adding additional parallel strings of converter cells.
The input characteristics of the $j^{th}$ and $k^{th}$ cells in a series string of $n$ cells for the modular architecture are governed by the following relationships

$$V_j = \frac{\eta_i P_i}{\eta_j P_j} V_i,$$

$$V_g = V_i \left(1 + \frac{\eta_i}{\eta_j} \sum_{j=1}^{n} P_j \right)^{-1},$$

$$I_s = \frac{P}{\sum_{j=1}^{n} \eta_j V_j},$$

where $I_s$ is the input current, $V_g$ is the input bus voltage, $V_i, V_j$ are cell input voltages, $P_i, P_j$ are cell output powers, and $\eta_i, \eta_j$ are cell efficiencies. The converter cells ideally act as constant power sinks in the input series string and transfer regulated power to the output LEDs. This behavior is shown in Fig. 2 with the input I-V characteristic for two cells, while more cells would have similar characteristics. The startup and breakdown regions represent operation below and above the rated voltages of the converter cells, $V_{\text{min}}$ and $V_{\text{max}}$, respectively. Unfortunately, this type of series converter operation is prone to instability, as shown in similar architectures [7-9]. At least one of the converter cells will always reach steady state outside of the desired operating region, which makes stabilization of the system the primary concern.

The main control objective, while ensuring stability of the system, is to have proportional input voltage sharing according to (1) while maintaining output current regulation of the series LEDs. Two significant differences in the LED system application compared to previous series architectures are that (1) the converter cell outputs independently drive floating LED loads and are thus not connected in series or parallel and (2) the output power or LED current regulation loop in each cell can be slow since it only has to respond to gradual variations due to temperature and aging.

Based on the characteristics mentioned above, there are two proposed control approaches: an autonomous open loop approach and a closed loop approach using inter-cell communication. The open loop approach requires no inter-cell communications, has a simple control implementation and a preset nominal operating mode. The closed loop solution achieves both stable input voltage sharing and independent output current regulation. The approach does require inter-cell communications, but maintains modularity with identical cells and communications are only preformed between neighboring cells to avoid isolation requirements.

**B. Open Loop Control Approach**

The open loop solution is based on having each converter cell behave as a constant loss-free resistor (LFR) [10] at its input port. This approach provides stability to the series converter string and ensures that each cell shares the input bus voltage proportional to its relative power in the system. The approach is termed “open loop” since the output current of each cell is not regulated. The converter cell may or may not have an internal feedback loop to achieve LFR behavior, depending on the converter topology and operating mode. One simple solution is to use a buck-boost converter operated in the discontinuous conduction mode (DCM) [10]. In this case, the averaged input resistance $R_e$ of the cell is a function of the duty cycle $D$ as given by

$$R_e = \frac{2L}{D^2 T_s},$$

where $L$ is the inductance and $T_s$ is the switching period.

Given nominal operating conditions, the cell duty cycles would be preset at the factory or calibrated by the user to generate the desired nominal LED output currents based on a specified number of cells and nominal input voltage $V_g$. The approach is simple and has several added benefits including the ability to dim the LEDs by scaling $V_g$ and inherent power factor correction (PFC) due to the resistor emulation of the input port. Drawbacks include the requirement for preset configuration and the inability to react to system variations such as changes in $V_g$, component values or LED failures.

**C. Closed Loop Control Approach**

The closed loop approach requires the converter cells to operate with two control loops in a similar fashion to PFC converters [10], as shown in Fig. 3. A fast inner loop, similar to the open loop approach, is used to achieve resistor emulation at the converter cell input port. The inner loop again provides stability to the series converter string and ensures proportional bus voltage sharing. A second slow outer loop with an integral type compensator is used to regulate the cell’s LED current or power. This approach ensures that the converter cells stabilize to the desired input voltage while remaining robust to changes in $V_g$ and regulating the LED current for improved light uniformity and LED failure response.

Since there are multiple competing loops within the system, it is necessary to consider system stability. If DCM buck-boost cells are again used to achieve near LFR...
behavior, then the desired duty cycle of a single series cell can be written as

$$D_1 = \frac{2L}{V_g T_s} \sum_{i=1}^{n_s} \eta_i P_i / \sqrt{\eta_i P_i},$$  \hspace{1cm} (5)$$

where $P_i$ is the cell output power. Given a nominal input bus voltage $V_g$ and assuming near identical cells with efficiency $\eta = \eta_i$, the duty cycle can be approximated as

$$D_1 \approx \frac{P_k}{P_1},$$  \hspace{1cm} (6)$$

where the constant $K$ is given by

$$K = \frac{2L \eta}{V_g T_s},$$  \hspace{1cm} (7)$$

and the total output power $P_{tot}$ is given by

$$P_{tot} = \sum_{i=1}^{n_s} P_i.$$  \hspace{1cm} (8)$$

In order to properly control the system, it is necessary to look at the potential change in duty cycle given the dynamics of the cell output power. This sensitivity function is given by

$$\frac{\partial D_1}{\partial P_1} = \frac{P_1 - P_{tot}}{P_1^{3/2}},$$  \hspace{1cm} (9)$$

which shows that the gain in the outer feedback loop will have a strong dependence on the total power $P_{tot}$ as well as the cell’s own power $P_i$. In fact the polarity of the sensitivity function changes when the power of a cell is equal to the total power of all other cells. For this reason, the knowledge of $P_{tot}$ is required to ensure the duty cycle is properly set.

The communication approach taken involves passing $P_{tot}$ among the cells in order for each cell to update its duty cycle corresponding to the received information. To maintain modularity in the system and avoid the cost and complexity of a system controller, a digital moving window average or chain control is adopted [11]. Each cell transfers in sequence the moving average of $P_{tot}$ to the next cell in the chain via a shared node according to

$$P_{tot,\text{prev}}[n] = P_{tot,\text{prev}}[n] - P_{tot,\text{prev}}[n-1] + P_{tot,\text{next}}[n].$$  \hspace{1cm} (10)$$

Figure 3 shows the LFR converter model with the closed loop control approach. The controller consists of three blocks, with a more detailed view shown in Fig. 4.

The current control block contains an integral compensator which takes the measured error between a reference and the output current and predicts the next desired output current. The output power can be approximated as a linear function of the output current when the converter cell is not in the startup or breakdown regions, therefore in closed loop the predicted output current is proportional to the predicted output power of the cell.

$$P_{tot,\text{prev}}[n] = P_{tot,\text{next}}[n] - P_{tot,\text{prev}}[n-1] + P_{tot,\text{next}}[n].$$  \hspace{1cm} (10)$$
This predicted output power $P_{\text{led}}[n]$ is then fed into the chain control block. A new total power $P_{\text{tot,prev}}[n]$ is calculated using the passed in total power $P_{\text{tot,prev}}[n]$ from the previous cell and the previous and current value for the predicted cell output power as given in (10). The new total power is then passed to the next cell in the chain.

The duty cycle generation block takes $P_{\text{led}}[n]$ and $P_{\text{tot,prev}}[n]$ from the chain control block and calculates the cell’s duty cycle from (6) using only one multiplication

$$D_i[n] = C_{\text{lookup}}[n] \cdot P_{\text{tot,prev}}[n], \quad (11)$$

and a lookup table (LUT) to find the constant $C_{\text{lookup}}[n]$ from its input $P_{\text{led}}[n]$ according to

$$C_{\text{lookup}}[n] = \frac{K}{\sqrt{P_{\text{led}}[n]}}, \quad (12)$$

In order to implement amplitude dimming with the closed loop algorithm, $K$ would need to be scaled with the input voltage $V_g$ which could be implemented with a LUT in order to avoid the need for sensing $V_g$. One simple way to implement LED failure mitigation would involve sensing a fault condition such as excessive average current or zero current. The converter cell could then short its input allowing no power to be transferred to the load while preserving continuity of the input current through the rest of the series string. The controller ensures that the remaining cells redistribute the input voltage while maintaining current regulation.

III. SIMULATION

A. Simulation Setup

For the modular architecture, the converter cell with resistor emulation was modeled in Simulink. Using the LFR model shown in Fig. 3 and a basic exponential model for the LED load, both control approaches were simulated. Because the chain control relies on sequential communication between cells, a discrete sampling algorithm was implemented. Using a communication sample time $T_s$ for the bottom cell, three offsets were created at

$$T_1 = T_s + \frac{T_s}{4}, \quad T_2 = T_s + \frac{T_s}{2}, \quad \text{and} \quad T_3 = T_s + \frac{3T_s}{4} \quad (13)$$

for each of the remaining three cells. There was also a specific startup procedure in the chain control to ensure a proper simulation. In this manner, each floating cell has ideal communication keeping the moving window accurate. Figure 5 shows the top level Simulink model implementation of chain control where the converter and compensator model of Fig. 3 is inside each cell block and input current $I_g$ is generated from the voltage across a source resistance $R_s$.

B. Open Loop Results

A simulation using the open loop control approach was performed to validate resistor emulation techniques and show the effects of dimming. The open loop simulation was implemented by ignoring the chain control information and setting the duty cycle inside the model to a fixed value. Four resistor emulator operated converter cells were series connected with fixed duty cycles. Amplitude dimming was then simulated by initializing a bus voltage at $V_g = 50$ V and then performing a step transition to $V_g = 40$ V. The simulations verified the four cells acted as resistors sharing the bus voltage and consequently decreasing output current appropriately when the bus voltage was reduced.

C. Closed Loop Results

Closed loop control of the system was also simulated with several goals: to verify stable input voltage sharing while maintaining output current regulation and to validate the ease of LED failure mitigation.

Four series connected cells were again simulated using the resistor emulator model but now with the chain control and integral compensator enabled. Figure 6(a) shows all four cells initially in regulation with 620 mA output current. Two successive transients were applied to cells 4 and 2 respectively. Both transients were applied via an LED reference current change to 402 mA. After applying the transient in both cases, the duty cycle of the applied cell increased to obtain the new regulated current and correspondingly, shown in Fig. 6(b), its emulated resistance decreased causing its share of the input voltage to decrease. Simultaneously, the other three cells’ input resistances increased, effectively regulating to the same output current.

A second simulation was performed to show LED failure mitigation. Assuming the cell could detect fault conditions (i.e. excessive currents or open circuit) and physically short its input, the simulation was created to show the resultant dynamics of the remaining cells. The transient in Fig. 7 shows the remaining three cells redistributing the input voltage and regulating their output currents. Table 1 gives the relevant DC operating points.
IV. EXPERIMENT

A. Experimental Setup

A prototype was developed to experimentally verify the modular architecture. The circuit employs the modularity of the architecture by having separable converter and load stages. Each cell is controlled via an onboard floating FPGA and corresponding sensing circuitry and ADCs. In order to power the FPGAs and other ICs reliably, two auxiliary DC-DC converters are driven by the cell input voltage with a UVLO that prevents operation below 6.3V on any cell. Given the power sink nature of the auxiliary converters, maintaining stability during startup is a challenge. A 100 \( \Omega \) resistor was placed across the cell input to stabilize the voltages during startup when the FPGAs were connecting to a CPU which was used for virtual I/O and logic analyzer functions only. Once the series string of converters reached a steady state open loop condition, their emulated resistances were much less than the 100 \( \Omega \) resistor negating its effect.

A four switch buck-boost power stage, as shown in Fig. 8, was implemented to test all three basic topologies (buck, boost, and buck-boost). A DCM buck-boost configuration was chosen in order to provide simple resistor emulation for the inner control loop, although...
average current [12], hysteretic [13] or nonlinear carrier control [14] methods could be used with a variety of topologies and operating modes to achieve the same result. Luxeon K2 700 mA emitters were used with a modular load configuration to test a variety of loads. A four LED load was chosen for each cell and the experiments covered an LED current range of 300 mA – 800 mA.

Each cell controller was implemented digitally in the floating FPGA, while an isolation IC was used to communicate between cells, validating the function of the system without a central global controller. A differential sensing circuit and an 8-bit ADC was used to convert the sensed output current. The main digital hardware for the controller itself was one LUT and one multiplier. A delay line based hybrid DPWM was used for the gate drive signal [15]. Figure 8 shows the prototype design and Table 2 gives details of the hardware used.

## B. Experimental Results

Many experiments were performed with this prototype using different topologies, operating modes and conditions. However, the two experiments shown in Figs. 9-10 validate the key aspects of the two proposed control approaches for this architecture. First, all four cells were run using the open loop control approach and DCM buck-boost power stages with four LEDs each. All four cells were initialized at a duty cycle that yielded approximately 620 mA output current given a bus voltage $V_g = 50$ V. Then amplitude dimming was tested by quickly decreasing the bus voltage to $V_g = 40$ V. Figure 9 shows that the four cells respond identically by decreasing their output current according to the decrease in input voltage.

A second experiment is shown in Fig. 10 which tested the closed loop control approach with two successive

**TABLE II - Power Switches and IC Components Used in Prototype**

<table>
<thead>
<tr>
<th>Device</th>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode</td>
<td>PDS540</td>
<td>Schottky 40V 5A</td>
</tr>
<tr>
<td>MOSFET</td>
<td>STN3NF06L</td>
<td>N-Channel 60V 4A</td>
</tr>
<tr>
<td>ADC</td>
<td>AD7825</td>
<td>8bit 4Channel Multiplexed</td>
</tr>
<tr>
<td>HB Driver</td>
<td>LM5101</td>
<td>Half Bridge Driver</td>
</tr>
<tr>
<td>Opamp</td>
<td>OPA350U</td>
<td>35MHz Rail-to-Rail</td>
</tr>
<tr>
<td>Isolator</td>
<td>ISO7221</td>
<td>Dual Digital Isolator 2MSPS</td>
</tr>
<tr>
<td>Boost</td>
<td>LT5436</td>
<td>Regulator 3A</td>
</tr>
<tr>
<td>Buck</td>
<td>LT3508</td>
<td>Dual Regulator 1.4A</td>
</tr>
</tbody>
</table>

**TABLE III - DC Operating Points for Experiments**

<table>
<thead>
<tr>
<th>Bus Input</th>
<th>Cell Input Voltage</th>
<th>Cell Output Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_g$ [V]</td>
<td>$I_g$ [A]</td>
<td>$V_1$ [V]</td>
</tr>
<tr>
<td>-----------</td>
<td>-------------------</td>
<td>-------------------</td>
</tr>
<tr>
<td>O.L. Dimming Fig. 9</td>
<td>Initial State</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>Final State</td>
<td>40</td>
</tr>
<tr>
<td>C.L. Transients Fig. 10</td>
<td>Initial State</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>Final State</td>
<td>50</td>
</tr>
</tbody>
</table>
small transients. The experimental results were obtained using the same conditions as the simulation from Fig. 6 and correspond well to the simulation results. When a transient change in the reference current occurred on one cell, it changed its duty cycle to regulate to the new value, while the remaining cells were able to maintain their current regulation with only a small perturbation. Table 3 contains the DC operating points of the experiment for both the open loop dimming test and the closed loop transient. The experimental results for the two consecutive transients closely match the simulation of the closed loop chain control architecture.

C. Observations

The experimental prototype was designed to be flexible and stable through many different testing conditions. The FPGAs were chosen to make control algorithm changes quick and to have the ability to synchronize with a CPU via JTAG communication for virtual I/O and logic analyzer capabilities. The JTAG communication is in a daisy chain structure and an isolation circuit was needed to connect all the FPGAs to the CPU. This communication with the CPU was not used to stabilize the system, but rather to provide simple monitoring and triggering of operating modes. The auxiliary converters used to power the FPGA, ADC, op-amp and drivers were also used to simplify the experimental process.

A potential commercial application is to integrate the control functions and power devices on a single low voltage IC. The only external components are the inductor and output capacitor, which can be minimized with high frequency operation of the low voltage cell. Each integrated cell would need only two control pins, one for sending signals up the chain and one for sending signals down the chain as well as the power stage pins. Isolators are not required for communications since control pins only connect to neighboring cells where current-mode techniques could be used to communicate over these overlapping nodes. A diagram of one option using a buck-boost converter power stage is shown in Fig. 11. The benefit when compared to one large high voltage converter is that many miniature, high efficiency, reduced voltage ICs are used. The only external components are the inductor and LED failure mitigation. Stability of the series converter string and independent regulation of the floating LED output currents are achieved using a two-loop controller that relies on chain control communications between cells to share system information. Simulation and experimental results demonstrate feasibility and operation of the architecture using series buck-boost converter cells. Both dimming and LED failure mitigation possibilities are enumerated and briefly examined as added benefits of the architecture.

V. CONCLUSION

The proposed series input modular architecture for LED lighting systems achieves the benefits of operating from a high bus voltage using low voltage converter cells with the flexibility to independently regulate the currents in small sub-strings of LEDs for improved light uniformity and LED failure mitigation. Stability of the series converter string and independent regulation of the floating LED output currents are achieved using a two-loop controller that relies on chain control communications between cells to share system information. Simulation and experimental results demonstrate feasibility and operation of the architecture using series buck-boost converter cells. Both dimming and LED failure mitigation possibilities are enumerated and briefly examined as added benefits of the architecture.

REFERENCES