Abstract — This paper proposes a digital output voltage sensing method for power factor correction (PFC) rectifiers that requires only a single analog comparator and a small amount of digital hardware. Using this method, a digital estimation of the output error voltage can be obtained at a rate of twice the line frequency \(2f_{\text{line}}\) without the use of a traditional analog to digital converter (A/D). The proposed method effectively implements a windowed A/D around the output reference voltage with a window range equal to the magnitude of the ac output voltage ripple. When used in combination with a nonlinear-carrier (NLC) current controller, a power feedforward function is inherently embedded in the operation of the single-comparator A/D (SCA/D), which simplifies the voltage loop design and reduces voltage loop gain variation due to operating power level. Experimental results are reported comparing load transient responses using the SCA/D or a traditional A/D in a digitally controlled 300W boost PFC.

I. INTRODUCTION

Many implementations of digital voltage loops for use in power factor correction (PFC) rectifiers have been proposed to either improve the dynamic response to line and load transients [1]–[3] or reduce the hardware complexity of a complete PFC controller [4], [5]. In all cases, the scaled output voltage \(H_v V_o\) or the scaled error voltage \(H_v V_e\) of the PFC stage was sampled using a medium resolution (8-10 bit) analog to digital converter (A/D). This paper proposes a new method for determining the digital value of the output voltage error signal using only a single analog comparator and a small amount of digital hardware. Throughout this paper, this method is referred to as the single comparator A/D (SCA/D).

In fully digital PFC’s such as in [1], [2], [6], the inductor or switch current is also sampled which typically requires a relatively fast A/D as sampling typically occurs at the converter switching frequency \(f_s\). This A/D is usually easily multiplexed to also measure the output voltage. However, in hybrid architectures PFC’s such as [3]–[5], [7], where the current loop is closed using analog techniques and the voltage loop is implemented digitally, the proposed technique eliminates the need for a traditional A/D altogether. Additionally, the proposed output voltage sampling technique retains the desirable qualities of a typical digital voltage loop such as the ability to implement a fast voltage loop [1]. Also, the proposed voltage loop inherently samples the output voltage synchronously at twice the line frequency \(2f_{\text{line}}\) which results in simpler digital voltage loop compensator design, allows for the avoidance of power command limit cycling as described in [8], and decreases input current total harmonic distortion (THD) by completely rejecting the output voltage ripple from the power command signal.

Fig. 1 shows a boost PFC stage with the proposed SCA/D and a digital voltage loop. The current loop may be of any type (digital or analog), \(C = 100\mu F\), \(L = 1.5\text{mH}\), \(V_o = 1/250\), \(V_{o,\text{nom}} = 385\text{V}\), \(f_s = 68\text{kHz}\).

This work has been sponsored through the Colorado Power Electronics Center (CoPEC)
outer voltage loop gain variation as power processing levels of the PFC stage change.

Section II describes the operation and characteristics of the SCA/D. The power feedforward feature of the SCA/D is discussed in Section III. Experimental results including waveforms of steady-state operation and verification of improved load transient response when the SCA/D is utilized to give a power feedforward gain are presented in Section IV. Section V concludes the paper.

II. SINGLE-COMPARATOR A/D (SCA/D) FOR VOLTAGE SENSING

Referring to Fig. 1, the output voltage \( V_o \), which has a significant ac ripple component due to the inherent instantaneous power imbalance between the PFC input and output over a half line cycle, is first scaled by a divider network \( H \) and then connected to a single analog comparator. The other comparator input is connected to a constant reference signal \( V_{ref} \) which sets the regulated output voltage set point. When the converter operates at or near regulation the waveform at the output of the comparator \( v_{comp} \) will be a square wave with a frequency of \( 2f_{line} \) and a duty cycle \( d_{comp} \) that is dependent on the specific dc value of \( V_o \). The output error voltage \( V_e \) is determined by the error voltage calculator block that consists of the required digital hardware to determine the duty cycle of the incoming \( v_{comp} \) signal over a period of \( 1/(2f_{line}) \) and relate the acquired duty cycle to a specific error voltage. The error voltage signal is then connected to a digital voltage loop compensator which outputs the power command signal \( u[n] \) which determines the amount of power being processed by the PFC stage.

A. Relationship Between \( d_{comp} \) and \( V_e \)

It is apparent that the SCA/D will only provide an accurate voltage measurement when the voltage sensing comparator is not saturated during an entire half line period. This reduces the sensing output voltage range to the peak-to-peak ac ripple voltage \( (2\Delta v_o) \). In effect, the proposed SCA/D creates a windowed sample of the output voltage centered around the steady state regulation point with a window range of \( \pm \Delta v_o \). One half of the peak-to-peak output voltage ripple can be found approximately as [14]:

\[
\Delta v_o \approx \frac{P}{4\pi f_{line}C V_{o,rms}}
\]

The ideal relation between \( d_{comp} \) and \( V_e \) is found as:

\[
V_e = \Delta v_o \sin((d_{comp} - 0.5)\pi)
\]

assuming that the output voltage ripple can be approximated as sinusoidal. This assumption is quite accurate as long as the PFC stage is capable of low THD rectification. As shown in (1), \( \Delta v_o \) is proportional to the operating power of the PFC stage and inversely proportional to the line frequency \( f_{line} \), the output capacitance value \( C \) and the rms output voltage \( V_{o,rms} \). Direct implementation of (2) would require that all these values be available for calculation of \( \Delta v_o \) and while \( f_{line} \) and \( V_{o,rms} \) are bounded in typical applications the remaining variables, which can be thought of in terms of \( \mu \mathrm{F}/\mathrm{W} \), vary greatly depending on the processing power of the stage during a particular operating period. In this paper there is no attempt made to determine \( \Delta v_o \) in (2) according to operating conditions so that \( V_e \) accurately represents the actual error voltage at any particular operating point other than during regulation (i.e. \( V_e = 0 \)). In fact, attempting to scale \( \Delta v_o \) with operating conditions would eliminate the power feedforward mechanism described in Section III. Furthermore, digital calculation of a sine relation, as in (2), typically requires a look-up-table resulting in a relatively large amount of hardware required to implement an equation. A simplified linear approximation of (2) with \( \Delta v_o \) replaced by a constant scalar \( V_K \) was investigated. This relationship is:

\[
V_e[n] = V_K [2d_{comp}[n] - 1]
\]

where the linearization was determined by simply making the relation between \( d_{comp}[n] \) and \( V_e[n] \) purely linear over the ranges of \( d_{comp}[n] = 0 \rightarrow 1 \) and \( \pm V_K \) respectively. The
magnitude of \( V_K \) sets the gain of the SCA/D and was chosen so that the gain of the linear estimation approximately matched the gain of the ideal SCA/D around regulation during full power operation (see Sec. III for details). This constant is found by:

\[
V_K = \frac{P_{\text{max}}}{8 f_{\text{line}} CV_{\text{o,rms}}} \tag{4}
\]

Fig. 2(a) shows the ideal relationship between \( d_{\text{comp}} \) and \( V_e \) for various power levels as well as the approximate linear relationship given by (3) with \( V_K = 16 \text{V} \) for the power stage shown in Fig. 1. As can be determined from the figure the error in measuring \( V_e \) can be quite large especially when the converter operates at lower power levels and \( V_e \) is not near zero. However, around regulation \( (d_{\text{comp}} = 0.5, V_e = 0) \) the linearly approximated SCA/D given by (3) reports an error voltage of zero regardless of the power processing level of the PFC stage. Also, with \( V_K \) chosen according to (4), it is apparent that the gain (slope) of the linearly approximated SCA/D matches the gain of the ideal SCA/D around regulation at rated power.

B. Implementation of the SCA/D

The implementation of (3) is inherently discrete and was accomplished entirely in digital hardware except for the single comparator and voltage reference shown in Fig. 1. Careful consideration was given to the implementation in order to minimize measurement errors while still achieving a simple solution requiring minimal digital hardware and a low frequency clock. The described implementation requires a total of 617 gates as reported from Xilinx ISE 8.2i and operates off a very low system clock frequency \( (f_{\text{sys}}) \) of 24.4kHz.

1) Debouncing \( v_{\text{comp}} \) and Generation of \( f_{\text{on}} \): As \( v_{\text{comp}} \) is the raw output of a comparator triggered on the output voltage, which contains not only ac ripple at 2\( f_{\text{line}} \) but also switching ripple at \( f_s \), debouncing of this signal is critical particularly in order to retrieve a power command update clock for the digital outer voltage loop \( (f_{\text{on}}) \) synchronous to \( 2f_{\text{line}} \). Generation of the debounced signal \( (v_{\text{comp}},d) \) is accomplished using a shift register approach similar to the debouncing described in [15]. The implemented shift register is 5-bits long which provides enough debouncing for operation at all power levels. The outer voltage loop clock is produced by generating a pulse of duration \( 1/f_{\text{sys}} \) every time \( v_{\text{comp}},d \) transitions from high to low. This creates a clock that is synchronous to \( 2f_{\text{line}} \) and power command updates that occur near the zero-crossings of the input voltage and current so that minimal input current distortion is realized. When the SCA/D is saturated, \( f_{\text{on}} \) is generated based on a minimum clock frequency of about 47Hz. This minimum clocking requirement allows the voltage loop to resume normal operation following an SCA/D saturation condition.

2) Calculating \( V_e[n] \): Two 8-bit counters are used to measure the effective on-time \( (t_{\text{on}}) \) and off-time \( (t_{\text{off}}) \) of the \( v_{\text{comp}},d \) signal. Both counters are reset on the falling edge of \( f_{\text{on}} \). The registers then increment depending on the state of \( v_{\text{comp}},d \). The \( t_{\text{on}} \) register increments when \( v_{\text{comp}},d \) is one and the \( t_{\text{off}} \) register increments when \( v_{\text{comp}},d \) is zero. An overflow of either counter results in the triggering of \( f_{\text{on}} \) as described above to maintain voltage loop clocking even during SCA/D saturation.

In order to minimize regulation offset errors, (3) is rewritten as:

\[
V_e[n] = V_K \left( \frac{t_{\text{on}}}{T} - \frac{t_{\text{off}}}{T} \right) \tag{5}
\]

where

\[
T = t_{\text{on}} + t_{\text{off}} = \frac{1}{2 f_{\text{line}}} \tag{6}
\]

Multiplication of (5) by \( T/T_{\text{max}} \) where \( T_{\text{max}} = f_{\text{sys}}2^n \) and \( n \) is the counter length results in the following relation that is easier to evaluate using digital hardware,

\[
\frac{T}{T_{\text{max}}} V_e[n] = V_K \left( \frac{t_{\text{on}}}{T_{\text{max}}} - \frac{t_{\text{off}}}{T_{\text{max}}} \right) \tag{7}
\]

where the raw values of the \( t_{\text{on}} \) and \( t_{\text{off}} \) registers are exactly equal to the ratios \( t_{\text{on}}/T_{\text{max}} \) and \( t_{\text{off}}/T_{\text{max}} \). Obviously \( V_e[n] \) is now scaled by a line-frequency dependent scalar that lowers the effective magnitude of the possible error voltage reported. This scalar is equal to 0.80 and 0.96 for line frequencies of 60 and 50Hz respectively. A digital phase locked loop (DPLL) could be implemented to produce a clock that had \( 2^n \) clock periods per half line cycle. This clocking arrangement would eliminate the above described line frequency gain dependency. Such a system was not implemented as the added line frequency dependent scalar did not greatly effect the performance of the outer voltage loop with an implemented SCA/D.

Fig. 2(b) shows the ideal SCA/D relation between \( d_{\text{comp}} \) and the digitally implemented relation as given by (7) for \( f_{\text{line}} = 60\text{Hz} \) and a 2V ideal quantization level of \( V_e[n] \) at rated power. Due to the frequency dependent scalar the maximum range of the reported error voltage is \( \sim 14\text{V} \) to 12V. Also, one can see that any \( v_{\text{comp}} \) duty cycle between 0.5 and about 0.6 will result in zero reported error. This is the zero error bin in terms of \( d_{\text{comp}} \).

![Fig. 3. Describing function of the SCA/D at different power levels and the describing function of a traditional A/D for reference](image-url)
### C. SCA/D Describing Function

A describing function is often used to describe the effective gain characteristics of nonlinear elements [16]. The sinusoidal describing function of the SCA/D for various power levels has been determined numerically by calculating the ratios of the fundamental components of the quantized A/D output and a sinusoidal input perturbation with swept amplitude. Fig. 3 shows the results of such a calculation for the SCA/D described in the above sections with $V_K = 16V$ and a 2V ideal quantization level. The describing function is shown for operating power levels of 300, 200, 100 and 50W and a line frequency of 60Hz. A describing function is also shown for a traditional A/D with 2V quantization.

As shown in Fig.3 the describing functions for the SCA/D display the affects of saturation of the converter particularly at lower operating powers. For the PFC stage parameters given in Fig. 1, the SCA/D begins to saturate at an error voltage of 10.3, 6.9, 3.4, and 1.7V for operating powers of 300, 200, 100 and 50W respectively. The saturation of the SCA/D results in a typical $1/x$ type response common to all saturated A/Ds.

### III. POWER FEEDFORWARD

One of the features of the SCA/D is that a power feedforward term is inherently embedded in its operation. The small signal gain of the SCA/D is described here to show how the gain is dependent on the operation power of the PFC stage. Referring to (3) the implemented SCA/D small signal gain ($\frac{\partial V_c[r]}{\partial d_{comp}[r]}$) is determined by linearizing the equation by differentiation and evaluating the result around the regulation point ($d_{comp}[n] = 0.5$). The implemented SCA/D gain is

$$\frac{\partial V_c[r]}{\partial d_{comp}[n]}|_{d_{comp}[n]=0.5} = 2V_K$$

(8)

Similarly the gain from $d_{comp}$ to actual error voltage ($V_{e,actual}$) is found by linearizing and evaluating (2) and then taking the reciprocal. The resulting gain is

$$\frac{\partial V_{e,actual}}{\partial d_{comp}}|_{d_{comp}[n]=0.5} = \frac{1}{\Delta v_o \pi}$$

(9)

Multiplying (8) and (9) together gives the complete SCA/D small signal gain from $V_{e,actual}$ to reported error voltage $V_c[n]$ as shown below,

$$\frac{\partial V_c[n]}{\partial V_{e,actual}} = \frac{2V_K}{\Delta v_o \pi}$$

(10)

Substitution of (1) for $\Delta v_o$ yields

$$\frac{\partial V_c[n]}{\partial V_{e,actual}} = \frac{8V_K f_{line} C V_{o,rms}}{P}$$

(11)

The above relation shows that the SCA/D has a small signal gain that is inversely proportional to the operating power of the PFC stage. This phenomena is also shown in the describing functions in Fig. 3. The average gain before saturation of the SCA/D describing function for operation at 300W is 0.8 due to the line frequency dependent scalar. At an operating power of 50W, six times lower than 300W, the SCA/D describing function shows an average gain roughly six times higher than at 300W resulting in a gain of about 4.8.

Careful selection of the current controller is necessary to realize a useful power feedforward mechanism. Table I shows the dc gain of the control-to-output transfer functions ($G_{vdc}$) for both the ACM and NLC current control approaches when modeled as an ideal rectifier [8]. The dc loop gain of the outer voltage loop ($T_{vdc}$) is also given in the table by multiplication of $G_{vdc}$, the voltage loop compensator dc gain ($G_{vc}$) and the SCA/D gain (11). Inspection of Table I reveals that the dc gain of ACM PFC architectures is inversely proportional to $P$ and that the dc gain of NLC architectures is proportional to $P$. Implementing the SCA/D with an ACM controlled stage results in increased voltage loop dc loop gain variation. This requires a compensator design that limits the attainable bandwidth across the operating power range of the voltage loop compared to if a traditional A/D was utilized. However, an NLC controlled PFC paired with the SCA/D results in a voltage loop dc loop gain that is fully compensated for variations in $P$ allowing a compensator design that reduces the amount of bandwidth variation across the operating power range. Futhermore, the power feedforward mechanism of the SCA/D paired with an NLC current controller is likely to be more effective at reducing overall voltage loop bandwidth variation at different operating points than an ACM controlled stage with the commonly implemented input voltage feedforward. This is due to the fact that the gain variation due to the rms input voltage residing anywhere in the universal input voltage range of 85 to 265V is about 10 whereas the power variation between full load and light load operation can be very large with a typical value being 20 when a PFC stage rated for 300W is operated at 15W for example.

### IV. EXPERIMENTAL RESULTS

A single 300W boost PFC prototype was built with specifications as shown in Fig. 1. The current loop controller for the prototype was capable of operating under either ACM or NLC control. The implemented digital voltage loop could be closed using either the SCA/D or a traditional 8-bit A/D.

#### A. Comparator Signal Conditioning and Clock Generation

Figure 4(a) shows the ac coupled output voltage and the accompanying comparator output ($v_{comp}$). In steady state the comparator output does show a duty cycle near 50% as expected. Also shown is the debounced version of $v_{comp}$, $v_{comp,d}$, with time periods $t_{on}$ and $t_{off}$ labeled. These signals

<table>
<thead>
<tr>
<th>Table I</th>
<th>CONTROL-TO-OUTPUT DC GAIN AND DC LOOP GAIN OF THE VOLTAGE LOOP WHEN THE SCA/D IS IMPLEMENTED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Controller</td>
<td>$G_{vdc}$</td>
</tr>
<tr>
<td>ACM</td>
<td>$\frac{V_{v,rms}^2}{2P}$</td>
</tr>
<tr>
<td>NLC</td>
<td>$-\frac{V_{v,rms}^2}{4V_{o,rms}^2}$</td>
</tr>
</tbody>
</table>

(results are for resistive load, no $V_o$ feedforward)
are shown in detail in Fig. 4(b) along with the 24.4kHz clock ($f_{sys}$) used to over-sample the comparator output via the $t_{on}$ and $t_{off}$ incrementing registers.

**B. Outer Voltage Loop Bandwidth Improvement**

The purpose behind implementing a power feedforward mechanism is to ultimately improve the line and load transient response of the outer voltage loop over a wide operating range. Fig. 5(a) shows the resulting loop gain and phase for the outer voltage loop with an implemented SCA/D for the PFC stage shown in Fig 1. The loop gain and phase is plotted for several operating power levels. Examination of this figure shows that the dc loop gain is constant for any operating power level. However, the cross over frequency and phase margin of the loop gain at different power levels are not the same. This is due to the movement of a pole in the ideal rectifier model that is dependent on the operating power of the stage. As the power of the PFC stage decreases the pole moves to lower frequency degrading both the outer voltage loop bandwidth and phase margin. For comparison Fig. 5(b) shows the loop gain and phase for an NLC controlled stage with a traditional A/D. Notice that the dc loop gains are now different as would be expected without a power feedforward implemented. Also notice that the overall bandwidth at lower operating powers is diminished compared to the NLC stage paired with the SCA/D. The voltage loop compensators implemented for the SCA/D and the traditional A/D loop gain plots are not identical but were designed so that both loop gains have the same bandwidth and phase margin at rated power. Table II summarizes the bandwidth and phase margin differences between the two outer voltage loops implemented with either the SCA/D or a traditional A/D. The bandwidth of the voltage loop implemented with the SCA/D is considerably improved at lower operating powers with the greatest demonstrated improvement being 3.7 times the bandwidth achieved with a traditional A/D at an operating power of 50W.

**TABLE II**

<table>
<thead>
<tr>
<th>$P_{load}$</th>
<th>SCA/D $BW_{CL}$</th>
<th>SCA/D $\Phi_M$</th>
<th>Trad. A/D $BW_{CL}$</th>
<th>Trad. A/D $\Phi_M$</th>
<th>$BW_{ratio}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>300W</td>
<td>6.53Hz</td>
<td>96°</td>
<td>6.52Hz</td>
<td>96°</td>
<td>1.0</td>
</tr>
<tr>
<td>200W</td>
<td>5.44Hz</td>
<td>86°</td>
<td>3.51Hz</td>
<td>80°</td>
<td>1.6</td>
</tr>
<tr>
<td>100W</td>
<td>3.94Hz</td>
<td>69°</td>
<td>1.57Hz</td>
<td>78°</td>
<td>2.5</td>
</tr>
<tr>
<td>50W</td>
<td>2.82Hz</td>
<td>53°</td>
<td>0.77Hz</td>
<td>71°</td>
<td>3.7</td>
</tr>
</tbody>
</table>

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Fig. 4. Waveforms showing steady state SCA/D operation and debouncing of $v_{comp}$ signal

Fig. 5. Loop gain and phase of the outer voltage loop of an NLC controlled PFC stage, $V_{g,rms} = 120V$, $f_{line} = 60Hz$
C. Load Transient Responses

Waveforms showing the ac coupled output voltage response to a 30W load transient at an initial operating power of 300W is presented in Figs. 6(a) and 6(b) for input voltages of 120V, 60Hz and 230V, 50Hz respectively. The current loop is under ACM control and an identical integral compensator was implemented for both of the voltage loops compared (closed with either a SCA/D or a traditional A/D). At an operating power of 300W the SCA/D gain is set according to (4) so the value of the reported error voltage ($V_e[n]$) is nearly equal to the actual error voltage ($V_e$). At both input voltages, the transient response is remarkably similar showing that under these conditions the SCA/D nearly replicates the operation of a traditional A/D.

A set of output voltage waveforms resulting from load transients for the NLC controlled PFC paired with the SCA/D is shown in Fig. 8. The output voltage waveforms resulting from various load transients are shown for a voltage loop closed using either the SCA/D or the traditional A/D. In this case, the voltage loop compensators in both implemented voltage loops are not identical but the resulting loop gains have the same bandwidth and phase margin at rated power as shown in Table II. Examination of Fig. 8 shows that voltage loop responses are similar at rated power but as the operating power decreases the voltage loop closed with a SCA/D begins to show an improved response. This improved response is due to the power feedforward mechanism of the SCA/D. As shown in Figs. 8(g) and 8(h), limit cycling of the outer voltage loop becomes an issue for the voltage loop closed by the SCA/D when operating at low power levels. This is due to the effective reduction of the zero-error bin voltage range of the SCA/D as operating power decreases. At 300W the zero-error bin is about 2.5V wide whereas at 50W the zero-error bin width has decreased to about 420mV, violating the limit cycle conditions described by [8]. Increasing the resolution of the power command signal using a $\Sigma-\Delta$ modulator, as in [6], is a possible solution to avoiding limit cycling when using a SCA/D without significantly increasing the required digital hardware to implement the digital voltage loop. Limit cycling aside, the action of the SCA/D voltage loop does return the output voltage to its dc regulation point more quickly than the traditional A/D at these low operating power levels.

The ac coupled output voltage waveforms resulting from a large load transient are shown in Fig 7. The effects of A/D saturation are apparent in the SCA/D waveform. The load transient is large enough that the error voltage is considerably larger than the maximum reported error voltage ($V_e[n]$) of 12V, resulting in SCA/D saturation. This saturation slows the voltage loop response considerably and while the voltage loop remains stable the peak output voltage and settling time both increase compared to the traditional A/D response. The transient waveform labeled $SCA_{D sat}$ shows the response of a SCA/D based voltage loop with an additional nonlinear feature designed to improve transient response. In this implementation, the maximum magnitude of $V_e[n]$ is increased by 10V when the SCA/D has been saturated (i.e. reporting maximum or minimum error voltage) for more than one half line period. As shown in Fig. 7, the settling time is improved to nearly match the performance of the traditional A/D. However, the peak output voltage value is not improved due largely to the one cycle delay required to detect saturation of the SCA/D. This delay results in the same peak output voltage value as with the standard SCA/D implementation.

![Fig. 6. Load transient comparisons between the SCA/D and a traditional A/D collected using the ACM controlled PFC in Fig 1](image)

![Fig. 7. Output voltage waveforms for a large load transient, $P = 300W \rightarrow 150W$, $V_g,rms = 120V, 60Hz$ for the NLC controlled PFC in Fig 1](image)
(a) Load transient responses for $P = 300W \rightarrow 250W \rightarrow 300W$, $V_{g,rms} = 120V, 60Hz$

(b) Load transient responses for $P = 300W \rightarrow 250W \rightarrow 300W$, $V_{g,rms} = 230V, 50Hz$

(c) Load transient responses for $P = 200W \rightarrow 170W \rightarrow 200W$, $V_{g,rms} = 120V, 60Hz$

(d) Load transient responses for $P = 200W \rightarrow 170W \rightarrow 200W$, $V_{g,rms} = 230V, 50Hz$

(e) Load transient responses for $P = 100W \rightarrow 85W$, $V_{g,rms} = 120V, 60Hz$

(f) Load transient responses for $P = 100W \rightarrow 85W$, $V_{g,rms} = 230V, 50Hz$

(g) Load transient responses for $P = 50W \rightarrow 40W$, $V_{g,rms} = 120V, 60Hz$

(h) Load transient responses for $P = 50W \rightarrow 40W$, $V_{g,rms} = 230V, 50Hz$

Fig. 8. Load transient waveforms comparing the performance of the SCA/D and a traditional A/D for the NLC controlled 300W PFC in Fig 1
V. CONCLUSIONS

This paper describes a digital output voltage sensing method for use with PFC rectifiers called the single comparator A/D (SCA/D). Using a single analog comparator and simple digital hardware it is possible to estimate the output error voltage within the range of the ac output voltage ripple. A full description of the operation of the SCA/D is given as well as analysis of the converters gain and describing function. It is further shown that the SCA/D provides a beneficial power feedforward mechanism when used in conjunction with an NLC controlled current loop PFC stage. Steady-state waveforms showing proper operation and outer voltage loop gain plots showing improved achievable bandwidth at lower operating powers are presented. Additionally, a comprehensive set of load transient responses for multiple input voltage and operating power conditions is shown for both the proposed SCA/D and a traditional A/D for comparison.

REFERENCES