Abstract—System modeling and digital control in a modular masterless multiphase architecture are presented in this paper. Two paralleled control loops, a voltage regulation loop and a current sharing loop, are designed for each phase. The paralleling structure allows both loops to have high bandwidth. Modeling of such systems shows that the voltage loops and current loops can be designed independently assuming identical power stages in each phase. Modeling also shows interaction between voltage and current loops if mismatches among phases are included. Voltage sensing mismatches among phases can result in competition between the two loops. Digital anti-saturation control approaches are proposed to avoid saturation of control loops and adaptively reach a steady state operating point which allows all loops to be active in the presence of voltage sensing errors among multiple voltage loops. Simulation and experimental results demonstrate the functionality of the proposed control method with a 2-phase 12 V to 1.5 V, 100 kHz per phase modular converter.

I. INTRODUCTION

Power supplies for high performance microprocessors must deliver low supply voltages with high currents while maintaining tight output voltage regulation in the presence of large load transients. Interleaved multi-phase converters are frequently used in such systems due to many advantages such as total current division among the phases, ripple cancellation, fast transient response and small output capacitance. In general, multi-phase converters require control approaches for current sharing among phases together with output voltage regulation.

Many approaches have been presented in the literature to control multi-phase converters [1-11]. Basic control structures can be summarized in the following three categories according to the relationship between current sharing loops and voltage regulation loops:

1) Outer voltage regulation loop and inner current sharing loops [1, 2], where a common voltage regulation loop is usually employed to provide a reference to current sharing control loops in each phase. Benefits of this structure include precise output voltage regulation and stable current sharing. Limitations include degraded modularity and poor fault tolerance.

2) Inner voltage regulation loops and outer current sharing loops [1, 3-7], where each phase has its own voltage sensing and voltage regulation, and outer current sharing loops adjust voltage references in each phase. This structure has better modularity, flexibility in system configuration and good fault tolerance.

3) External controller structure, where a dedicated controller is used to perform current sharing and voltage regulation. Almost all digital control approaches proposed for multi-phase converters are based on external digital master controllers [8, 9]. This structure can result in good current and voltage regulation, but it has poor modularity and requires large amount of interconnections between each phase and the external controller, such as voltage sensing, current sensing and gate drive signals, which impact noise coupling and system reliability, as well as system size and cost.

This limitation from poor expandability and large amount of interconnections will become increasingly important in future microprocessor power supplies, where the rapidly increasing supply current requirements are expected to drive the number of required phases up. This provides a motivation for exploration of alternative masterless multi-phase architectures with improved scalability to an arbitrary number of phases.

In this paper, a digitally controlled masterless multi-phase structure based on identical DC-DC converter modules that communicate over a digital bus [10], as shown in Fig. 1, is studied. The advantages of the masterless architecture include simpler system configuration, scalability to an arbitrary number of phases, redundancy, potentials for reduced noise and improved reliability by short sensing and driving connections, and reduced system cost based on identical digitally controlled modules.

Digital control design for the architecture shown in Fig. 1 is proposed in this paper, together with system modeling and mismatch consideration. A pair of paralleled voltage regulation and current sharing loops is designed for each...
module. System modeling results show that the two loops are decoupled if power stages in each phase are identical. With mismatches among phases considered, there will be interaction between voltage and current loops. Digital anti-saturation control approaches are presented to avoid saturation of control loops and guarantee a steady state operation with all loops active in the presence of voltage sensing non-idealities among multiple voltage loops.

In this paper, a digital control structure designed for the masterless multi-phase architecture is described in Section II, followed by system modeling results in Section III. Impacts of voltage sensing non-ideality to operation of control loops are discussed in Section IV. Then anti-saturation control approaches are proposed in Section V to resolve the problems caused by voltage sensing errors. Section VI presents experimental verification on a digitally controlled two-phase 12 V to 1.5 V buck converter.

II. CONTROL STRUCTURE IN MASTERLESS MULTI-PHASE ARCHITECTURE

A two-phase digitally controlled modular masterless multi-phase buck converter is shown in Fig. 2. This system is easily expandable to an arbitrary number of phases. Each module is composed of a power stage (synchronous buck converter), a digital controller, and analog to digital interface components. The digital controller performs digital voltage regulation, current sharing control, soft start and digital pulse width modulation.

In a masterless multi-phase system, each phase has an independent voltage regulation loop and a current sharing solution has been presented in [10]. In this paper, we focus on the cooperation between voltage regulation and current sharing regulation in each phase, as well as multiple loops in all phases.

The control structure proposed in this paper is to connect the two loops in ‘parallel’ in each phase, rather than traditional inner / outer loop dependencies. In each phase, duty ratio control is applied. The duty cycle command \( d \) used to drive the power stage is a combination of two parts:

\[ d = d_v + d_i \]

as shown in Fig. 2. \( d_v \) is generated by the voltage regulation loop based on sensed voltage error \( v_e = v_{ref} - v_c \), and \( d_i \) is generated by the current sharing loop based on current error \( i_e = i_{ave} - i_L \). Similar structure in analog control can be found in [11].

For inner/outer loops structure, the speed of the outer loop is usually limited by the inner loop. The parallel structure allows both loops to be designed independently with high bandwidth. But paralleled structure also introduces the potential of competition between loops.

III. MODELING OF A MODULAR TWO-PHASE BUCK CONVERTER

A. System loop gains

System modeling is studied to obtain insight of overall system behavior and provide controller design guidelines. Figure 3 shows the overall system model for a two-phase masterless multi-phase converter with control loops as shown in Fig. 2. \( C_v \) and \( C_i \) are the voltage loop compensator and the current loop compensator, respectively. Power stages are modeled as control-to-output transfer functions.

Due to the paralleling structure of voltage and current loops, it is not obvious which loop could represent the overall performance and stability of the system. Ideally, current sharing regulation should not affect output voltage and vice versa. So these two loops are considered individually first.

1) Voltage regulation only:

Assume there are only voltage loops and perturb at the input of voltage loops, a voltage loop gain \( T_v \) can be obtained:

\[ T_v = \frac{v_v}{v_x} = C_v \cdot (G_{vd1} + G_{vd2}) \] (1)

2) Current regulation only:

Assume there are only current loops and perturb at the input of current loops, a current loop gain \( T_i \) can be obtained:

\[ T_i = \frac{i_v}{i_x} = C_i \cdot (G_{id1} + G_{id2}) \]
\[ T_i = \frac{v_i}{v_x} = K \cdot C_i \cdot (G_{vd1} + G_{vd2} - G_{id1} - G_{id2}) \] (2)

With interactions between voltage and current loops considered, “overall” system loop gains can be obtained in a similar way.

3) Voltage regulation considering effects of current loops:

Perturb at the input of voltage loops and consider the effects of both loops, overall loop gain by perturbing the voltage loop \( T_{sys(v)} \) can be obtained:

\[ T_{sys(v)} = T_v = \frac{C_v \cdot \left( \frac{K}{2} \cdot C_i \cdot (G_{vd1} - G_{id1}) \cdot (G_{vd2} - G_{id2}) \right)}{1 + T_i} \] (3)

4) Current regulation considering effects of voltage loops:

Perturb at the input of current loops and consider the effects of both loops, overall loop gain by perturbing the current loop \( T_{sys(i)} \) can be obtained:

\[ T_{sys(i)} = T_i = \frac{C_v \cdot \left( \frac{K}{2} \cdot C_i \cdot (G_{vd1} - G_{id1}) \cdot (G_{vd2} - G_{id2}) \right)}{1 + T_v} \] (4)

Due to space limitation, the derivation of above transfer functions will be disclosed in future publications.

B. Discussion and compensator design

Comparing (1) and (3), we can see if \( G_{id1} = G_{id2} \), or \( G_{vd1} = G_{vd2} \), then \( T_{sys(v)} = T_v \). That is to say, if the power stages of the two phases are identical, then current loop compensators and duty ratio-to-current transfer functions have no effect to the voltage regulation. Similarly, comparing (2) and (4), \( T_{sys(i)} = T_i \) if power stages are identical. One conclusion can be drawn that voltage regulation and current sharing regulation are decoupled in this system if the power stages of each phase are identical.

From (3) and (4), we can see power stage mismatches will cause interaction between voltage regulation and current sharing regulation. The interactions are dependent on the mismatches, the designed voltage loop compensator \( C_v \) and current loop compensator \( C_i \). It is hard to design \( C_v \) and \( C_i \) based on \( T_{sys(v)} \) and \( T_{sys(i)} \) directly.

So for compensator design purpose, we can assume the power stages are identical, and design the voltage loop compensator and the current loop compensator based on \( T_v \) and \( T_i \), respectively. Then overall system loop gains \( T_{sys(v)} \) and \( T_{sys(i)} \) should be used to verify system stability and performance considering worst case power stage mismatches.

In a single loop system, there is only one overall system loop gain representing system stability and performance. But in a masterless multi-phase system, there are multiple inputs/outputs and multiple control loops. Voltage loops are regulating voltage errors to zero, while current loops are regulating the current difference between the two phases to zero. Voltage regulation has no control to the current difference. So in such systems, there are two overall system loop gains and both of them should be stable to ensure the entire system stability.

C. Compensator design example

Compensators are designed for a 12 V-to-1.5 V 2-phase synchronous buck converter with 100 kHz switching frequency per phase. The nominal parameter values are: \( L_1 = L_2 = 1.0 \mu H \), \( R_{i1} = R_{i2} = 20 \, m\Omega \), \( C_1 = C_2 = 3 \, mF \) and \( R_c = 1 \, m\Omega \). This system is also used for simulation and experiment in this paper.

With nominal parameters, voltage and current compensators were designed based on (1) and (2) separately. The designed crossover frequency of \( T_v \) is 10 kHz, and that of \( T_i \) is 10 kHz. Both voltage loop and current loop have high bandwidth. Assume worst case mismatch in the system to be \( L_1 = 0.5 \mu H \), \( R_{i1} = 30 \, m\Omega \), \( L_2 = 2.0 \mu H \), \( R_{i2} = 10 \, m\Omega \). \( T_{sys(v)} \) and \( T_{sys(i)} \) were obtained based on (3) and (4), respectively.

![Compensator design example](image-url)
Figure 5(a) shows $G_{v_1}, T_1$, and $T_{y_1(0)}$ and 5(b) shows $G_{v_2}, T_2$, and $T_{y_2(0)}$. From Fig. 5 we can see $T_1$ and $T_{y_1(0)}$, $T_2$, and $T_{y_2(0)}$, are very close to each other. The designed bandwidth and phase margin will not be highly degraded with mismatch considered.

IV. IMPACT OF VOLTAGE SENSING ERRORS

In the masterless multi-phase converter shown in Fig. 2, each voltage loop senses the voltage at the output of each module ($v_{c_1}$ or $v_{c_2}$) and compares them to an on-board reference voltage ($V_{ref_1}$ or $V_{ref_2}$) independently. Voltage errors seen by each phase are likely to be different because of any differences in physical sensing points (e.g. different $R_w$’s) and reference voltages.

If both voltage regulation loops are working actively, they should regulate the DC values of $v_{c_1}$ and $v_{c_2}$ to be

$$V_{c_1} = V_{ref_1}, V_{c_2} = V_{ref_2}.$$  \hspace{1cm} (5)

If current sharing loops are working actively, they should regulate the DC inductor currents identical: $I_{c_1} = I_{c_2}$. Thus DC output currents should also be identical:

$$I_{o_1} = I_{o_2}.$$ \hspace{1cm} (6)

From Fig. 2,

$$V_{c_1} = R_{w_1} \cdot I_{o_1} + V_o, \hspace{0.5cm} V_{c_2} = R_{w_2} \cdot I_{o_2} + V_o$$ \hspace{1cm} (7)

must be satisfied. Then (5) and (6) can not be satisfied at the same time if $V_{ref_1} \neq V_{ref_2}$ and/or $R_{w_1} \neq R_{w_2}$. Thus when voltage sensing errors appear among voltage loops, there will be no steady state operating point for all voltage and current loops to be active. Also, competition among loops will appear in this case and it will continue until one or more loops become saturated, as shown in Fig. 5.

Simulation shown in Fig. 5 was performed in the system described in Section III C. Non-ideality is modeled by different wire resistances $R_{w_1} = 5 \text{ m} \Omega$ and $R_{w_2} = 1 \text{ m} \Omega$, while reference voltages are identical $V_{ref_1} = V_{ref_2} = 1.5 \text{ V}$. Total load current is 30 $\text{ A}$.

Voltage loops and current loops in the two phases compete from start up and no steady state can be reached when all loops are active. If two load currents were identical, then $V_{c_1}$ would be larger than $V_{c_2}$. If $V_{c_1} = V_{c_2}$, $I_{o_1}$ would be smaller than $I_{o_2}$. So, during competition, $V_{c_1}$ tends to be higher than $V_{c_2}$, $V_{c_2}$ tends to be lower than $V_{c_2}$, and $I_{o_1}$ tends to be smaller than $I_{o_2}$. So in phase I, $v_{c_1} < 0$, $v_{c_1} > 0$ and $d_{v_1}$ kept decreasing, $d_{v_1}$ kept increasing. Until $d_{v_1}$ reached its lower limit: $d_{v_1} = 0$ and stayed in saturation. In phase II, $v_{c_2} > 0$, $i_{c_2} < 0$ after start up, so $d_{v_2}$ kept increasing and $d_{v_2}$ kept decreasing until voltage loop in phase I lost control. In steady state, voltage loop in phase I was saturated: $v_{c_1} \neq 0$; and all other loops were active $I_{o_1} = 0$, $I_{o_2} = 0$ and $i_{c_2} = 0$.

In steady state, the output voltage can be regulated by the phase with an active voltage loop and the two inductor currents can be shared by the two active current loops. This results in valid steady-state operation, but during transient, the saturated voltage loop cannot respond when it needs to decrease the duty cycle further. So the transient performance will be largely degraded since it is designed to have the two voltage loops working together.

Thus the speeds of $d_v$ or $d_i$ increasing / decreasing during competition depend on the magnitude of voltage sensing errors and the bandwidth of voltage and current loops. If fast voltage and current loops are designed, competition speed will be fast and one or more loops will go to saturation in a short time.

Which loop(s) goes to saturation depends on the upper / lower limit settings of $d_v$’s, $d_i$’s, the steady state duty ratio $D$ and the magnitude & polarity of voltage sensing errors. In simulations and experiments in this paper, duty ratio generated by a voltage loop is limited by $0 \leq d_v \leq 1$ and duty ratio generated by a current loop is limited by $-0.5 \leq d_i \leq 0.5$. The steady state duty ratio is $D = 0.125$.

If $d_v$ limit is small, current loops can go to saturation first, and thus currents can not be shared after saturation. If $D$ is above 0.5 and limit settings are the same as above, the voltage loop with increasing output $d_v$ (e.g. phase II in Fig. 5) will go into saturation first.

If a multi-phase system has above limit settings and steady state duty ratio, only one of the voltage loops will stay active and all current loops can stay active in the steady state. As in the two-phase case, steady state operation can be ok, but voltage regulation during transient will be degraded and designed regulation speed can not be achieved.

Digital anti-saturation control approaches were developed and are discussed in the next section to keep all voltage loops and current loops active in steady state, in the presence of voltage sensing errors among phases.

V. DIGITAL ANTI-SATURATION CONTROL APPROACHES

From Section IV, voltage sensing errors among phases cause the following problems:

(I) There is no DC operating point allowing all loops to be active; and

(II) Control loops can go to saturation and stay in saturation without recovery.

To resolve these problems, digital variables can be controlled in each phase and effective voltage reference also can be adjusted digitally. Two complementary anti-saturation
control approaches are proposed below: magnitude control approach and \( V_{ref} \) adjustment control approach.

### A. Magnitude control approach

Magnitude control approach is developed to confine the magnitudes of \( d_i \)'s and \( d_i \)'s in a certain range, so that voltage and current loops will never go into saturation.

The duty cycle command \( d \) controlling power stage operation is the sum of voltage loop output \( d_c \), and current loop output \( d_i \), and \( d \) themselves are both internal variables in the digital controller in each phase and their individual values are invisible to the power stage. In an ideal system (no mismatches), \( d \) is usually very small and \( d \) is the dominant part in \( d \). Voltage loops and current loops will not go into saturation if we can always keep \( d_i \) small and \( d \) dominant.

Figure 6 shows the idea of magnitude control approach. A bound \( \pm \Delta \) is set to the magnitude of \( d \). If \( d \) goes beyond this bound, it is adjusted back to 0 and at the same time \( d \) is adjusted by the same amount, but in the opposite direction, to keep the sum \( d \) unchanged. Power stage operation will not be affected by such adjustment. Dotted lines in Fig. 6 show \( d_i \)'s and \( d_i \)'s in no magnitude control case and \( d_i \) in phase I goes into saturation in steady state. With magnitude control approach, both loops will never go into saturation.

If only magnitude control is applied, two loops will always compete. During competition, all voltage errors and current errors are non-zero, which means output voltage is not well regulated and inductor currents are not shared. It is desired to find a steady state operation condition with zero voltage & current errors and all regulation loops active. \( V_{ref} \) adjustment control approach is design to accomplish this goal.

### B. \( V_{ref} \) adjustment control approach

\( V_{ref} \) adjustment control adaptively searches a steady state operating point that allows all loops to be active.

From (7), we can see that with given \( R_{w1}, R_{w2} \) and \( V_{ref1} \), there exists a desired \( V_{ref2} \) that allows (5) and (6) to be satisfied at the same time. That is to say, if we keep one \( V_{ref} \) constant and adjust the other one, a steady state operating point with all loops active can be found. In multiple phase converters, this statement should also stand. If we keep one arbitrarily picked \( V_{ref0} \) constant and other phases adjust their \( V_{ref} \) individually, steady state operation with all loops active can be achieved.

The theoretical value of the desired reference value in one phase can be derived from (7) assuming (5) and (6) are true:

\[
V_{ref,\text{desired}} = V_{ref0} \cdot \frac{1 + \frac{R_{w1}}{N \cdot R}}{1 + \frac{R_{ref0}}{N \cdot R}}
\]

where \( N \) is the number of phases and \( R \) is the load resistance. Equation (8) shows: 1) there exists and exists only one desired \( V_{ref} \) for each phase in a certain condition; 2) the desired \( V_{ref} \) value in each phase is dependent on load. After a load transient, each phase may need to readjust its \( V_{ref} \).

Desired \( V_{ref} \) values need not be computed by (8) by the digital controller. Following effective search algorithm is proposed to find them adaptively.

In a multiple phase system, one \( V_{ref0} \) is picked arbitrarily to be constant. All other phases adjust their effective \( V_{ref} \)'s by a digital \( \Delta V_{ref} \) to reach their desired values individually. A \( d_i \) going beyond the given bound is treated as a sign of competition. If a \( d \) in one phase goes beyond the bound once, a digital \( \Delta V_{ref} \) in this phase will be adjusted once by one step. As shown in Fig. 6, \( \Delta V_{ref2} \) is always 0 and \( \Delta V_{ref} \) is adjusted digitally. The adjustment step can be 1 LSB of the output voltage sensing.

Theoretical value of \( \Delta V_{ref} \) in phase \( i \) is

\[
\Delta V_{ref} = V_{ref,\text{desired}} - V_{ref_i},
\]

where \( V_{ref_i} \) is the on-board reference voltage of phase \( i \).

\( \Delta V_{ref} \) can go positive and negative and effective reference voltage in each phase is the sum of on-board analog \( V_{ref} \) and this digital \( \Delta V_{ref} \). The search will continue until a steady state operating point is obtained. Then all voltage and current loops can be active in steady state without competition.

The size of magnitude adjustment bound \( \Delta \) affects the time length needed for \( V_{ref} \) adjustment control. If \( \Delta \) is large, it takes longer for a \( d \) to reach it, so that it takes longer for a \( \Delta V_{ref} \) to adjust one step. \( \Delta \) can not be too small either, or transient \( d \) response may trigger \( \Delta V_{ref} \) adjustment.

If only \( V_{ref} \) adjustment control is applied to a system (other search scheme is needed), the adjustment would have to be completed before any loops reach saturation. With high bandwidth voltage and current regulation, saturation can happen fast. It is very hard to guarantee no saturation operation. So, both the magnitude and \( V_{ref} \) adjustment control approaches are needed to ensure all loops active in the steady state.

### C. Simulation verification

Figure 7 shows simulation results in the same system as in Fig. 5 with anti-saturation control approaches. \( V_{ref2} \) is kept constant, and \( V_{ref} \) is adjusted adaptively.

![Fig. 6: Anti-saturation control approaches.](image-url)
At the starting part, voltage and current loops in the two phases were competing to each other, and magnitude control was working to confine $d_1$'s and $d_2$'s away from saturation. Each time $d_1$ was adjusted, $V_{\text{ref}1}$ was also adjusted by 1 LSB of output voltage sensing by the $V_{\text{ref}1}$ adjustment control. A steady state operating condition was reached after 3 steps of $V_{\text{ref}1}$ adjustment. Note that all loops remain active both during competition and steady-state, and all $d_1$'s and $d_2$'s are stable in steady-state.

VI. EXPERIMENTAL VERIFICATION

Experimental verification was performed in a 2-phase synchronous buck converter with 100 kHz switching frequency per phase. Input voltage is 12 V, output voltage is 1.5 V and full load current is 12 A. The nominal inductance value for each phase is $L = 1.0 \, \mu\text{H}$ and the output capacitance is $C = 3 \, \text{mF}$. THS1230 A/D converter is used for voltage and current sensing. Inductor currents are sensed through the on-resistance of the synchronous rectifiers. Voltage and current compensators were designed as shown in Fig. 4. A field programmable gate array (FPGA) based digital controller using a Xilinx Virtex II evaluation board was used to implement the functionality of the two digital controllers and the communication between them. Further details of the experimental test circuit can be found in [12].

Figure 8 shows experiment results with minimized mismatches between the two phases. Load connections and on-board voltage references of the two modules were made identical. In this case, mismatches were very small and invisible in the digitized voltage errors. We can see that output current regulation was very fast and currents were distributed evenly after transient.

In experimental results shown in Figs. 9, 10 and 11, mismatches were built between the two phases: $V_{\text{ref}1} = 1.50 \, \text{V}$, $V_{\text{ref}2} = 1.50 \, \text{V}$, $R_{s1} = 3 \, \text{m}\Omega$ and $R_{s2} = 7 \, \text{m}\Omega$. The voltage sensing zero-error bin is 15.6 mV and current sensing bin is about 0.5 A. $V_{\text{ref}2}$ was kept constant and $\Delta V_{\text{ref}2}$ was subject to change by the anti-saturation control approaches.

Figure 9 shows the current sharing performance of the two phase converter. When the current sharing enable signal was low, current sharing loops were disabled. The load current is 3 A total, so that voltage sensing errors caused by different load connection resistances were too small to be seen by the voltage loops. After the enable signal turned high, the current loops were regulating the currents to be identical.

Experimental waveforms shown in Fig. 10 were a start-up process to 11 A load current in the two-phase buck converter. The output voltage had soft-start controlled by the digital controllers. With 11 A load current, voltage sensing errors can be seen by the two voltage loops. We can compute the theoretical value of desired $V_{\text{ref}2}$ and $\Delta V_{\text{ref}2}$ by (8) and (9): $V_{\text{ref}2,\text{desire}} = 1.5217 \, \text{V}$ and $\Delta V_{\text{ref}2} = 21.7 \, \text{mV}$. So the loops were competing after start up and currents were not shared during competition.

Figure 11 shows experimental data captured by ChipScope Pro Logic Analyzer from the FPGA at the same time when an oscilloscope captured Fig. 10. Data were stored once per single phase switching period, which was 10 $\mu\text{s}$. We can see the competing $d_1$ and $d_2$ in each phase after start up. We can see Phase I performed magnitude control at about 90 cycles and Phase II did at about 115 cycles. When phase II performed magnitude control, its $\Delta V_{\text{ref}2}$ was adjusted by

![Fig. 7: Simulation for magnitude control and Vref adjustment control approaches in a 2-phase buck converter with different wire resistances from each phase to the load](image1)

![Fig. 8: Experimental results of a load transient from 3 A to 11 A in a two phase buck converter with paralleled voltage and current regulation and minimized voltage sensing errors.](image2)

![Fig. 9: Experimental current sharing performance of the modular masterless 2-phase buck converter with proposed control approaches.](image3)
1 LSB of voltage sensing. After \( \Delta V_{vref} \) was adjusted, two phases could not see voltage sensing error anymore. Two phase currents were controlled to be identical after that and all loops stayed active in steady state.

Simulation and experimental results demonstrated the good performance of proposed control structure and anti-saturation approaches.

VII. CONCLUSIONS

System modeling and digital control in the modular masterless multi-phase architecture are presented in this paper. Two paralleled control loops, a voltage regulation loop and a current sharing loop, are designed for each phase. The paralleling structure allows both loops to have high bandwidth. Modeling of such systems shows that the voltage loops and current loops can be designed independently assuming identical power stages in each phase.

Modeling also shows interaction between voltage and current loops if mismatches among phases are included. Voltage sensing mismatches among phases can result in competition between the two loops. Advanced control approaches are proposed to avoid saturation of the control loops and adaptively reach a steady state operation point which allows all loops active in the presence of voltage sensing errors among multiple voltage loops.

Simulation and experimental results with a 2-phase modular masterless multi-phase converter demonstrate the functionality of the proposed control method.

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