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Practice Quiz 2

ECEN 4517/5517

Spring 2016

Assume that the MSP430F5172 processor has been configured as follows:

- Watchdog timer is disabled
- Processor clock frequency is 25 MHz
- Timer D clock frequency is 200 MHz

Write complete code that accomplishes the following:

- Timer D switching frequency of 100 kHz
- Read logic input on pin P1.1
If the input is high, then select a duty cycle of 50%. If the input is low then select a duty cycle of 0.
- Use Timer D to produce this duty cycle and switching frequency on PWM output P1.7
- Other PWM outputs should be turned off
- Remove otherwise unnecessary commands