

VITA

ANDREW R. PLESZKUN

OFFICE ADDRESS

Department of Electrical and Computer Engineering
University of Colorado - Boulder
425 UCB
Boulder, CO 80309-0425
Phone: (303) 492-3571 or (303) 492-7327
email: arp@colorado.edu

PERSONAL DATA

Date of Birth: December 7, 1955
U.S. Citizen by Birth

EDUCATIONAL RECORD

University of Illinois: Ph.D. degree in Electrical Engineering, August 1982.
University of Illinois: Masters of Science Degree in Electrical Engineering, May 1979.
The Illinois Institute of Technology: Bachelor of Science Degree in Electrical Engineering, May 1977.
Institut Nationale Des Science Appliquees De Lyon, Villeurbanne, France. I.N.S.A. has an exchange program with I.I.T. through which a student may spend his junior year in France. The courses taken at I.N.S.A. were all taught in French and the classes taken with the French students were equivalent to those which would have been taken at I.I.T.

RESEARCH INTERESTS

Computer architecture, VLSI design of high performance computers, storage hierarchies/cache organization, optical computing and VLSI design for optical systems, digital system design with Verilog.

WORK EXPERIENCE

8/07-Present - Associate Chair for Education, Electrical and Computer Engineering, University of Colorado - Boulder.
8/94-7/07 - Associate Professor, Electrical and Computer Engineering, University of Colorado - Boulder.
5/94-8/94 - Acting Chair, Electrical and Computer Engineering, University of Colorado - Boulder.
1/94-5/94 - Acting Associate Chair, Electrical and Computer Engineering, University of Colorado - Boulder.
8/88-12/93 - Associate Professor, Electrical and Computer Engineering, University of Colorado - Boulder.
8/82-8/88 - Assistant Professor, Computer Sciences Department, University of Wisconsin-Madison.

GRANTS AND AWARDS

Bruce Holland Teaching Excellence Award, 2005.
NSF Grant, "Memory Prefetching," co-PI: Dirk Grunwald, 6/97-5/00, (\$450,000).
Undergraduate Excellence Fund Award, "Expansion and Upgrade of the ECEN 2830 (Digital I) Laboratory," with W. M. Waite and J. Avery, Fall 1997, (\$10,400).
Undergraduate Excellence Fund Award, "A VLSI Systems Design Laboratory," Fall 1996, (\$25,000).
DOC Grant DASG60-91-C-0143, "Optical Multi-Processor Interconnect," (co-PI: Joh Sauer, H. Jordan),

10/91-9/93, (\$313,088).

CALSPAN - UB Research Center Grant No. F306702-88-D-0026, "Development of an Optical Serial Arithmetic Unit," 6/89, (\$90,997).

President's Junior Teaching Scholar

NSF Grant CCR-8706722, "Architectures of High Speed List Processing," (co-PI: Guri Sohi), 8/87-6/90, (\$315,920)

NSF Grant DCR-8604224, "High Performance Computing in VLSI/ULSI," (co-PI: James R. Goodman), 6/86-11/88, (\$468,766).

NSF Grant DCR-8202952, "Decoupled Access/Execute Computer Architectures for VLSI/USLI," (co-PI: James R. Goodman), 8/84-8/86.

1983 IBM Faculty Development Award Recipient, (\$60,000 award).

Co-PI on NSF Equipment Grant, "Instrumentation and Equipment to Support the Design, Prototyping and Debugging of VLSI Systems," 6/83, (\$150,000).

NSF Grant ECS-8207277, "Decoupled Access/Execute Computer Architectures," (co-PI: James E. Smith), 11/82-4/86.

PROFESSIONAL and HONOR SOCIETIES

Association for Computing Machinery

Institute of Electrical and Electronics Engineers

TEACHING AND CURRICULUM DEVELOPMENT

Developed the VLSI Systems Design course (ECEN 4109/5109). This development also included obtaining a equipment donation of 12 workstations from HP to build a CAD Lab for instructional use. Over the years these equipment has been upgraded through College Engineering Excellence Grants.

Developed ECEN 1400 - Introduction to Digital and Analog Electronics.

Migrated the ECEN 2120 Computers as Components from an Intel x86 platform to a Motorola 68000-based platform.

INTEGRATED CIRCUITS DEVELOPMENT

The PIPE processor chip, a 32-bit nMOS processor. This processor was fabricated through the MOSIS facility and ran with a 5.5 MHz clock.

In conjunction with this project I established a lab to test fabricated chips. Other chips that we had successfully produced included an ALU and datapath chip and a chip with hardware data queues.

PUBLICATIONS

A. R. Pleszkun, B. R. Rau, E. S. Davidson, "An Address Prediction Mechanism for Reducing Processor-Memory Address Bandwidth," *Proc. 1981 IEEE Workshop on Computer Architecture for Pattern Analysis and Image Database Management*, Nov. 11, 1981.

A. R. Pleszkun, "A Structured Memory Access Architecture," CSG Report No. 10, Coordinated Science Laboratory, University of Illinois, Urbana, Illinois, August 1982.

- "PIPE: A High Performance VLSI Architecture", *Proceedings of the Workshop on Computer Systems Organization*, New Orleans, LA, March 1983.
- A. R. Pleszkun and E. S. Davidson, "A Structured Memory Access Architecture," *1983 International Conference on Parallel Processing*, Bellaire, MI, August 1983.
- J. R. Goodman, J. Hsieh, K. Liou, A. R. Pleszkun, P. B. Schechter, H. Young, "PIPE: A Decoupled Architecture for VLSI," *The 12th Annual International Symposium on Computer Architecture*, June 1985.
- J. E. Smith, A. R. Pleszkun, "Implementation of Precise Interrupts in Pipelined Processors," *The 12th Annual International Symposium on Computer Architecture*, June 1985.
- J. Hsieh, A. Pleszkun, M. Vernon, "Performance Evaluation of a Pipelined VLSI Architecture using the Graph Model of Behavior (GMB)," *IFIP 7th International Symposium on Computer Hardware Design Languages and their Application*, August 1985.
- G. Bier, A. Pleszkun, "An Algorithm for Design Rule Checking on a Multiprocessor," *22nd Design Automation Conference*, June 1985.
- A. R. Pleszkun, G. Sohi, B. Kahalleh, E. Davidson "Features of the Structured Memory Access (SMA) Architecture," *COMPCON 86* March 1986.
- A. R. Pleszkun and M. K. Farrens, "An Instruction Cache Design for Use with a Delayed Branch," *Advanced Research in VLSI: The 4th MIT Conference*, April 1986.
- A. R. Pleszkun and M. J. Thazhuthaveetil "An Architecture for Efficient LISP List Access," *The 13th Annual International Symposium on Computer Architecture*, June 1986.
- A. R. Pleszkun and M. J. Thazhuthaveetil "The Architecture of Lisp Machines," *Computer Magazine*, March 1987.
- G. Craig, J. Goodman, R. Katz, A. Pleszkun, K. Ramachandran, J. Sayah, J. Smith, "PIPE: A High Performance VLSI Processor Implementation," *Journal of VLSI and Computer Systems*, Vol. 2, Nos. 1 & 2, 1987.
- A. R. Pleszkun and M. J. Thazhuthaveetil "On the Structural Locality of Reference in Lisp List Access Streams," *Information Processing Letters*, Elsevier Science Publishers B.V. (North-Holland), October 19, 1987.
- A. R. Pleszkun, J. R. Goodman, W. C. Hsu, R. T. Joersz, B. Bier, P. Woest, and P. B. Schechter, "WISQ: A Restartable Architecture Using Queues," *The 14th Annual International Symposium on Computer Architecture*, June 1987.
- A. R. Pleszkun and G. Sohi, "The Performance Potential of Multiple Functional Unit Processors," *The 15th Annual International Symposium on Computer Architecture*, June 1988.
- J. E. Smith, A. R. Pleszkun, "Implementation of Precise Interrupts in Pipelined Processors," *IEEE Transactions on Computers*, Vol. 37, No. 5, May 1988, pp. 562-573.
- M. K. Farrens and A. R. Pleszkun, "Improving Performance of Small On-Chip Instruction Caches," *The 16th Annual International Symposium on Computer Architecture*, June 1989.
- M. K. Farrens and A. R. Pleszkun, "An Evaluation of Functional Unit Lengths for Single Chip Processors," *Proceedings of the 23rd Annual Symposium and Workshop on Microprogramming and Microarchitectures*, November 1990.
- A. R. Pleszkun and M. J. Thazhuthaveetil, "Architectural Features of Lisp Computers," Chapter 2, *Computers for Artificial Intelligence Processing*, Edited by B. W. Wah and C. V. Ramamoorthy, John Wiley & Sons, Inc. 1990.
- M. K. Farrens and A. R. Pleszkun, "Implementation of the PIPE Processor," *Computer*, January 1991.

- M. K. Farrens and A. R. Pleszkun, "Details of the PIPE Processor Implementation," *Proceedings of the 1991 Hawaii International Conference on System Sciences*, Kapaa, Kauai, January 1991.
- M. K. Farrens and A. R. Pleszkun, "Strategies for Achieving Improved Processor Throughput", *The 18th Annual International Symposium on Computer Architecture*, June 1991.
- G. Tyson, M. Farrens and A. Pleszkun, "MISC: A Multiple Instruction Stream Computer", *The 25th Annual International Symposium on Microarchitecture*, Portland, Oregon, December 1992.
- M. K. Farrens, G. Tyson and A. R. Pleszkun, "A Study of Single-Chip Processor/Cache Organizations for Large Numbers of Transistors," *The 21st Annual International Symposium on Computer Architecture*, April 1994.
- A. R. Pleszkun, "Techniques for Compressing Program Address Traces," *The 27th Annual International Symposium on Microarchitecture*, December 1994.
- G. Tyson, M. Farrens, J. Matthews, and A. Pleszkun, "A Modified Approach to Data Cache Management", *The 28th Annual International Symposium on Microarchitecture*, Ann Arbor, Michigan, April 1995.
- G. Tyson, M. Farrens, J. Matthews, and A. Pleszkun, "Managing Data Caches using Selective Cache Line Replacement", *International Journal of Parallel Programming*, Vol. 25 No. 3, pg 213-242, June 1997.
- D. Grunwald, A. Klauser, B. Manne and A. Pleszkun, "Confidence Estimation for Speculation Control", *The 25th Annual International Symposium on Computer Architecture*, June 1998.
- John L. Metz, Andrew R. Pleszkun, Kristina M. Johnson, "CMOS smart photosensor array for optoelectronic hit/miss transform processing of cervical smears", in LEOS'98 Conference Proceedings, Vol. 2, p. 67-68, Orlando, Florida, Dec. 1-4, 1998.
- John L. Metz, Andrew R. Pleszkun, Kristina M. Johnson, "CMOS smart pixel array to complete an optical hit/miss transform algorithm", *1998 OSA Annual Meeting*,
- Stephen Aiken, Dirk Grunwald, Andrew Pleszkun and Jesse Wilke, "A Performance Analysis of the iSCSI Protocol," *IEEE Mass Storage Conference*,

Graduate Advisor

Professor Edward S. Davidson, Dept. of EECS University of Michigan, Ann Arbor, MI.