High-Efficiency Amplifiers for Portable Handsets

Thomas Mader, Milica Marković, Zoya B. Popović
University of Colorado, Boulder, CO
Reza Tayrani
Compact Software, Paterson, NJ

Abstract – **Achieving high-efficiency in rf and microwave amplifiers is important for reducing the size and weight, and increasing the output power, battery lifetime and reliability of portable wireless transmitters. Here we present a switched-mode high-efficiency transmission-line amplifier circuit with a measured 80 % power-added efficiency (PAE) with 0.55 W at 0.5 GHz, and 73 % PAE with 0.94 W at 1 GHz from a single Siemens CLY5 MESFET. At 5GHz from a Fujitsu FKL052WG, 0.61 W was obtained with 72 % power added efficiency and 81 % drain efficiency. First-order design equations adequately predict the amplifier behavior.**

1. Introduction

By increasing the efficiency of a 50% efficient amplifier to 90%, the dissipated heat power is reduced by a *factor of nine* for the same output power. Therefore, the heat-sink mass is reduced significantly. Or, if the heat-sink size is kept the same, the output power is increased significantly. Increasing the efficiency of high-power circuits will decrease their size and power consumption, and increase their output power, reliability and lifetime.

Currently, microwave amplifiers have demonstrated 71% power-added efficiency (PAE) at 1.75 GHz with 1 W of power [1], 75.8 % at X-band [2] with 0.6 W, and around 35 % at Ka band [3] with 0.7 W of power. At microwave frequencies, several classes of amplifier operation are commonly used [4]. In class A, the transistor operates as a linear amplifier, i.e. a gain can be defined. Since the transistor is ON during the entire RF period, the theoretical efficiency is limited to 50 %. In class B amplifiers, the dc bias point is adjusted so that the transistor is ON during half of the cycle, and in rf and microwave amplifiers the other half of the waveform is obtained from a tank circuit. The amplifier has a theoretical maximum efficiency of 78.6%. In class C operation, the bias point is adjusted so that the transistor conducts only during a small part of the rf cycle, resembling pulsed operation. In class E or D amplifiers, the transistor operates as an ON/OFF switch, and assuming the switch is ideal, the theoretical efficiency is 100 %. Class D employs two transistors that work as a switch pair with a tuned resonant circuit at the output. In class D amplifiers both transistors can be on or off at the same time during the switching transient therefore reducing efficiency at the higher frequencies. These problems are solved by using single-ended amplifiers, class F and Class E. Transmission-line type Class F amplifiers have a theoretical efficiency of 100 %. Class F has higher maximum output power than class E. The disadvantage of class F is that it has to present a short circuit exactly at the transistor output making the construction of the output circuit difficult. At low RF frequencies, class E amplifiers exhibit as high as 96 % efficiency [5]. More background information about the different power amplifier classes is given in reference [4].

At microwave frequencies, transistors are far from ideal switches. We demonstrate modified class-E switched-mode amplifiers with microwave transistors by using their parasitic capacitances as part of the amplifier circuits. In these amplifiers, the input CW signal drives a transistor operating as a switch. Even though the voltage across the transistor itself is not sinusoidal, the tuned output circuit is designed to produce a sinusoidal voltage across the load. The challenge in obtaining high efficiency lies in the design of the tuned circuit such that the current and voltage transistor waveforms produce minimal dissipation in the active device. When there is a voltage across the output transistor terminals, there is no current flow through the device (and vice versa), so the IV product is ideally zero, corresponding to 100 % DC-to-RF conversion efficiency.

High-efficiency amplification is important for portable wireless handsets, and the presented amplifiers provide the following advantages:

- more RF output power from any transistor, which directly translates to higher data rates: for every 3 dB increase in power, the data rate increases by a factor of 2;
- reduced heat-sink size because of reduced heat dissipation;
- reduced mass since higher efficiency correlates directly to less power dissipation, and therefore reduced heat-sink size;
- longer battery lifetime;

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- good modulation characteristics (e.g. low parasitic AM), as well as adequate bandwidth for high data rate communications.

2. Design Procedure

The class-E circuit shown in Fig.1a can be analyzed exactly by solving a fifth-order set of nonlinear differential equations. The solutions are transcendental equations which can be solved numerically if a good starting point for the values is known. This analysis does not allow design of the circuit for a given transistor and gives no insight into its operation. Therefore, optimization for efficiency is not practical in this case. We have developed a first-order design procedure with the following approximate method. The results can then be used as a starting point for a detailed analysis, when needed. The external *RLC* network has a high Q-factor and resonates slightly below the switching frequency f_s, so that the voltage across the output port R is constrained to be a sinusoid. Another effect of the high-Q filter LC section is to constrain the current through L to also be approximately a sinusoid at the switching frequency (plus the dc supply current I_g). These assumptions simplify the basic explanation of the class-E circuit significantly.

Since the current flowing into the external load network is sinusoidal, it can be replaced with an equivalent current source. The transistor switch can be either ON or OFF. When the switch is turned ON, there is no voltage across the switch, but a piece of sinusoidal current (with a DC component) flows through it. During the OFF interval, the equation for the switch voltage v_s is

$$C_s \frac{dv_s}{dt} = I_g(1 - a\sin(\omega_s t + \phi)).$$

The latter can be integrated with the following boundary conditions:

$$v_{C_s}(0) = 0, \quad v_s(\frac{T_s}{2}) = 0 \quad \text{and} \quad \frac{dv_s}{dt}(\frac{T_s}{2}) = 0.$$

These constraints determine a and ϕ uniquely:

$$a = \sqrt{1 + \frac{\pi^2}{4}} \simeq 1.862 \quad \text{and} \quad \phi = -\tan^{-1}\frac{2}{\pi} \simeq -32.48^\circ.$$

Note that these are constants for *any* high-Q class-E circuit with a capacitor in shunt with the switch (any microwave class-E circuit, for example). Now the voltage and current through the load network v_{net} and i_{net} are known:

$$v_{net}(t) = \frac{I_g}{\omega_s C_s}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi))$$

$$i_{net} = I_g(a\sin(\omega_s t + \phi) - 1).$$

It is of interest to find the relationship between V_g and I_g, or in other words, how much current is drawn for a given

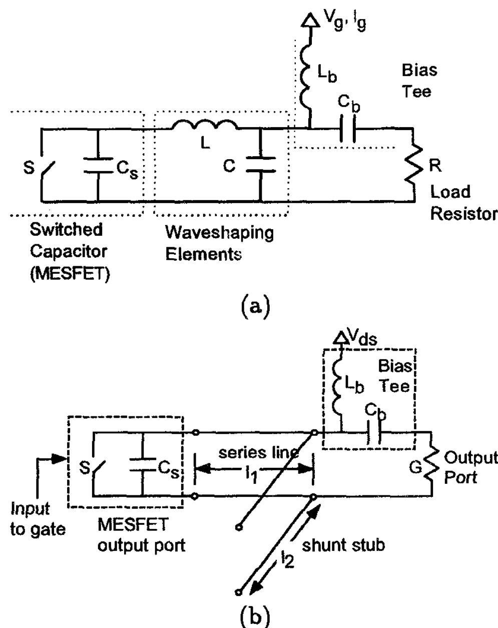

Figure 1: (a) Standard low-frequency class-E topology with lumped elements. (b) Modified class-E topology for microwave/millimeter-wave applications. The microwave transistor is represented as a switched capacitor.

supply voltage or vice-versa. V_g is the dc component of $v_{net}(t)$, the voltage across the switch, capacitor and load network. The following is obtained after taking the time-average of the voltage:

$$I_g = \pi\omega_s C_s V_g.$$

This rather simple result has important implications for a practical microwave class-E circuit, assuming that the minimum value of C_s must necessarily be the parasitic capacitance of a microwave device, for example C_{ds} of a MESFET. For example, at a specified frequency, a device with some output capacitance C_s must operate well above the knee voltage, say 2 volts. Since ω_s, C_s, and V_g are now specified, one hopes that the device can handle the required maximum current, which is $(1+a)I_g \simeq 2.86 I_g$! If the device can not handle this current, then it is *impossible* to make an ideal class-E circuit with the particular device at that frequency.

At microwave and millimeter-wave frequencies, transmission lines are often preferred over lumped elements because lumped elements are much lossier and more difficult to fabricate. Fig.1b shows the series/shunt transmission-line class-E circuit. L_b and C_b act as a bias tee, but are assumed not to affect the RF operation of the circuit appreciably. Both transmission lines are assumed to be between 0° and 90° long.

The class-E conditions described above are applied to the

load network (admittance is used here for simplicity) [8]:

$$Y_{net} = \frac{\omega_s C_s}{k_0} e^{-j\theta_0}, k_0 \simeq 0.28015, \theta_0 \simeq 49.0524^\circ.$$

The shunt section of transmission line looks capacitive at the switching frequency, and can be replaced by an equivalent capacitor C (its length is less than 90°). A numerical solution using standard transmission-line equations gives a value of C and the line length l_1. In current practice, transmission line lengths $\beta_1 l_1$ and $\beta_2 l_2$ from Fig.1b are usually determined using experimental load-pull techniques or harmonic-balance circuit simulations, without insight into the operation of the circuit. The design formulas based on the high-Q assumption give a first-order high-efficiency output match for a microwave transistor, and give insight into the operation of high-efficiency microwave amplification.

3. Measurements

The Siemens CLY5 MESFET was used in a microstrip transmission-line circuit. The layout of the circuit is shown in Fig.2. The methodology of the design is briefly described in [6]. In the lab, the device (whose output capacitance is 2.6 pF), was heavily saturated, and the input and output circuits were adjusted experimentally until the maximum PAE was obtained. A maximum PAE of 80% was measured at 0.5 GHz at an output power of 550 mW and a gain of 15.3 dB. The measured drain efficiency was 83%. After this performance was experimentally obtained, a series inductance was included in the transistor switch model; this inductance appears between the switched capacitor and the series transmission line in Fig.1b, and can be compensated for. From an equivalent circuit device model (Materka) and microwave CAD analysis, the inductance was estimated to be 1.7 nH. This modified transistor output port model was used in the later designs.

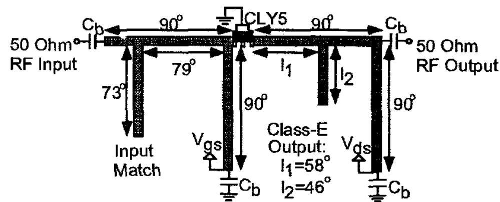

Figure 2: Design and layout of the class-E microstrip circuit. Bias to the Siemens CLY5 MESFET is brought in through quarter-wave shorted stubs. A Duroid substrate is used, with a thickness of 100 mils and $\epsilon_r = 10.5$.

The microstrip layouts of the 1.0 and 2.0 GHz class-E circuits using the Siemens CLY5 look similar to the 0.5-GHz microstrip circuit shown in Fig.2. No adjustments were done on the output circuit in these two cases; only the input circuit was adjusted for minimum return loss.

For the 1-GHz amplifier, drain efficiency and power-added efficiency are plotted as a function of frequency in Fig.3a. The maximum PAE is 73 % at 1 GHz with 0.94 W of output power, 14.7 dB gain and a 75% drain efficiency. The efficiency is high over a broad frequency range. The power-added efficiency is greater than 65% over a 12% bandwidth. Output power, drain efficiency and power-added efficiency are plotted as a function of input power level in Fig.3b. The efficiency is high over a broad input power range; however, the output power is mostly constant over this range. Therefore, this class-E circuit is well-suited for frequency modulation because the amplitude stays constant when the frequency is varied.

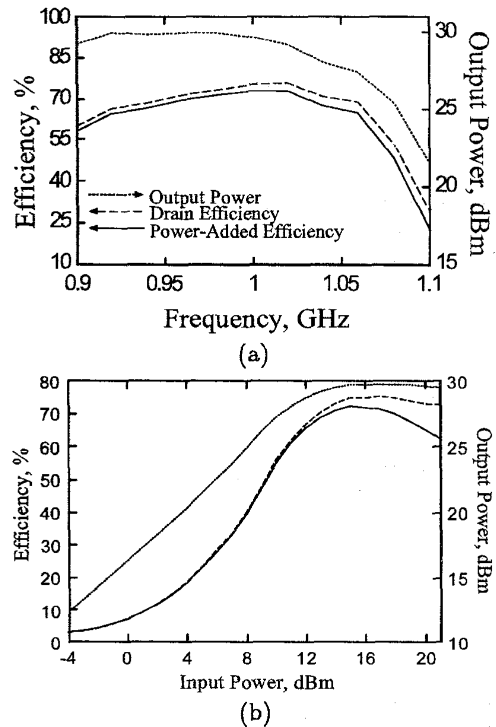

Figure 3: (a) Power-added-efficiency (solid line) and drain efficiency (dashed line) of the 1.0 GHz CLY5 class-E amplifier as a function of frequency under large-signal gate drive conditions. (b) Output power (dotted line), power-added efficiency (solid line), and drain efficiency (dashed line) as a function of gate input drive level for the 1.0 GHz CLY5 class-E amplifier.

The dc power level of the ideal class-E circuit is proportional to the switching frequency if the supply voltage and switch capacitance are held constant:

$$P_{dc} = \pi \omega_s C_s V_g^2.$$

For the 0.5-GHz CLY5 class-E circuit, the DC power level was 666 mW. For this 1.0 GHz CLY5 class-E circuit, the

DC power level is 1244 mW. The ratio between the two power levels is 1.87; in the ideal case, the ratio should be 2.

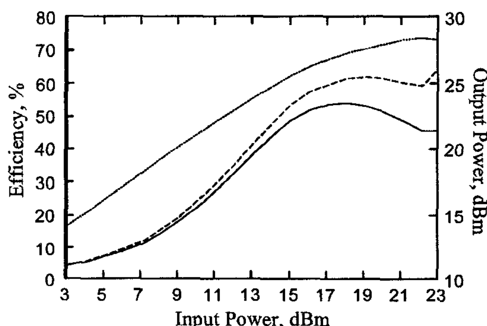

Figure 4: Measured drain efficiency and power-added efficiency are plotted as a function of input power level for the 2-GHz amplifier.

For the 2-GHz amplifier, drain efficiency and PAE are plotted as a function of input power level in Fig.4. The maximum PAE is 54% at 2 GHz with a corresponding power of 0.53 W and 9.1 dB of gain. The maximum drain efficiency is 62%. The simplified analysis described above gives a maximum frequency of class-E operation for a given transistor's output capacitance and maximum current-carrying capability, I_{max}:

$$f_{max} = \frac{I_g}{2\pi^2 C_s V_g} = \frac{I_{max}}{2\pi^2(1+a)C_s V_g} \simeq \frac{I_{max}}{56.5 C_s V_g},$$

where $a \simeq 1.8621$. For the class-E circuits considered here, the supply voltage is 6 V, and the output capacitance was found to be about 2.6 pF. From the data sheets, the maximum drain current for the Siemens CLY5 is approximately 1.2 A (when the gate voltage is slightly positive). This yields a maximum frequency of "ideal" class-E operation of approximately 1.4 GHz. Therefore, the 2.0-GHz class-E circuit presented here operates in a "suboptimal" class-E mode. The class-E circuit demands a higher peak drain current than the MESFET can provide. This explains why the output power level is much lower than expected at this frequency, and why the efficiency drops so suddenly between the switching frequencies of 1.0 GHz and 2.0 GHz.

A 5 GHz class-E microstrip amplifier was also designed, fabricated and tested. The circuit looks similar to the one shown in Figure 2 and uses a Fujitsu FKL052WG MESFET. At 5 GHz, the amplifier exhibits 10dB of compressed gain (4dB into compression) with a saturated output power of 0.6 W, a power added efficiency of 72 % and a drain efficiency of 81 %. The power added efficiency was greater than 70 % over a 5 % bandwidth, and greater than 60 % over a 10 % bandwidth. These results show that the first-order simple design theory is a good starting point for high-efficiency amplifier design.

4. Acknowledgements

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