INTERNATIONAL JOURNAL OF NUMERICAL MODELLING: ELECTRONIC NETWORKS, DEVICES AND FIELDS
*Int. J. Numer. Model.* **12**, 157–170 (1999)

# Incorporating non-linear lumped elements in FDTD: the equivalent source method

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SUMMARY

A new approach is presented for modelling three-dimensional lumped elements in the finite-difference time-domain (FDTD) solution of Maxwell's equations. The finite-difference equations for the lumped element's circuit behaviour are derived to produce discrete relationships between the device's terminal currents and voltages. These difference equations are then implemented in the FDTD grid with equivalent voltage and current sources based on static field approximations. The method can be used for a wide range of applications which include lumped elements that may be passive, active, linear, non-linear, single, and multiple port devices. The underlying advantages of modelling a lumped element in this manner as compared to the more traditional extended FDTD technique is that the lumped element is easily extended across multiple FDTD cells and the need for a separate transcendental equation solver is eliminated. The method is demonstrated by a specific example based on the Curtice–Cubic non-linear model for a MESFET. The s-parameters from an FDTD simulation are compared to the manufacturer's measured data and to results from simulations using Hewlett-Packard's Microwave Design System (MDS). Finally, the method is used to model the MESFET in a three port oscillator. Copyright © 1999 John Wiley & Sons, Ltd.

## 1. Introduction

The common method to incorporate lumped element devices in FDTD has been the extended FDTD formulation [1–3] in which a lumped current term has been added to the differential form of Ampere's law:

$$\nabla \times \bar{H} = \varepsilon \frac{\partial \bar{E}}{\partial t} + \bar{J}_{\mathrm{C}} + \bar{J}_{\mathrm{L}} \tag{1}$$

The current is split into two contributions: the conduction current density, $J_{\mathrm{C}}$, and the current density due to the lumped circuit element, $J_{\mathrm{L}}$. The lumped circuit element's current density is a function of the voltage developed across the element. Thus the voltage–current relationship of the element may be used to formulate $J_{\mathrm{L}}$ in terms of the electric field in the direction of the device orientation. Algorithms based on this method for simple elements such as the resistor, capacitor, and inductor yield semi-implicit, numerically stable equations. However, the inclusion of a semiconductor pn junction required by a transistor results in a set of coupled non-linear

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CCC 0894–3370/99/010157–14$17.50

transcendental equations that must be solved at each time step.[4] Thus an additional procedure for solving non-linear equations must be employed such as the Newton–Raphson approach. In addition, in order to increase computational efficiency and ensure the convergence of the procedure, a time-step adaptive algorithm may be used.[5] However, elimination of the separate non-linear solver would be ideal.

Furthermore, there have been modifications to the extended FDTD method to model lumped elements that span more than one FDTD cell.[6,7] The first method[6] yields an electric update equation that is considerably more complex than that of the original extended FDTD algorithm. It was also noted that the method was unstable for structures with small permittivity.[7] The second, more stable, solution requires an LU matrix decomposition and back-substitution for its solution. The matrix size of this modified method increases as the square of the number of cells that is spanned by the lumped element.

A new approach, the equivalent source lumped element method, substitutes approximately equivalent sources in place of the lumped elements. This eliminates the need for a separate non-linear equation solver and easily allows the lumped element to be extended across multiple FDTD cells without increasing complexity or computational requirements.

## 2. The equivalent source method

In general, the method proceeds according to the flowchart in Figure 1. First, the current is found from the FDTD grid at the device terminals. Then the circuit equations are used to find the voltage across the device terminals. Finally, the voltage is implemented in the FDTD grid as an electric field source. Depending on the particular device or circuit being modelled, it may be advantageous to interchange the roles of the voltage and the current. In that case, the voltage is computed based on the electric fields in the FDTD grid. Then the current through the lumped element is calculated from the device's circuit equations and implemented in the FDTD simulation by an equivalent magnetic field source.

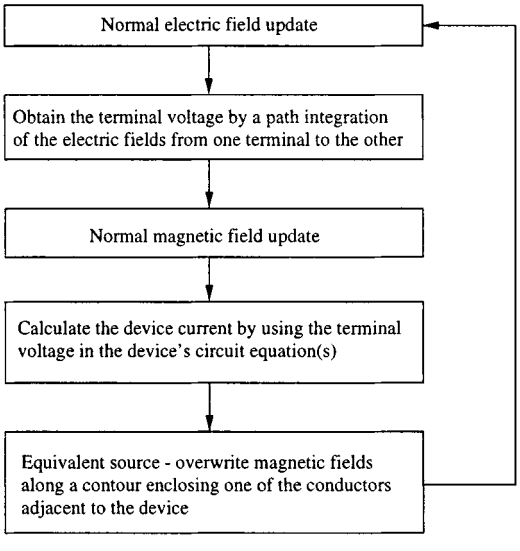


Figure 1. Flowgraph of the equivalent source lumped element method

 

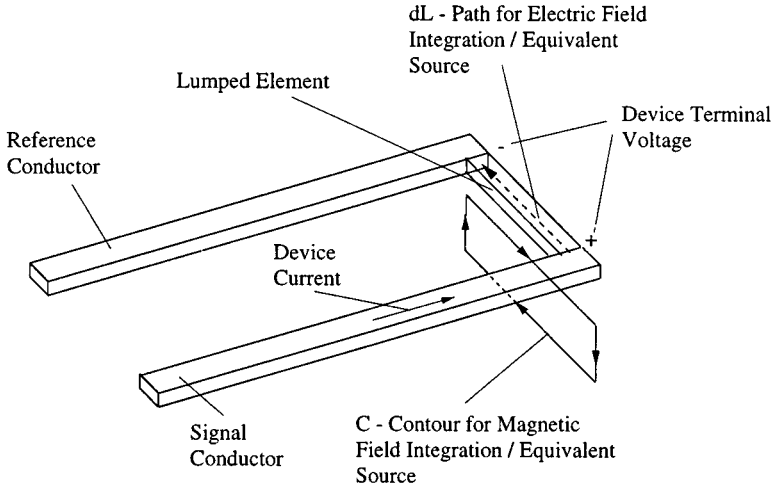


Figure 2. Example layout of lumped element device placed across two conductors

For most applications, the lumped element is positioned with its terminals placed such that it is across two conductors. An example layout is shown in Figure 2. In order to calculate the terminal voltage or current, it is necessary to define the direction of the current flow through the device and the orientation of the voltage potential across the terminals. These definitions are arbitrary, but must be consistent with the device's circuit equations.

For example, suppose that the lumped element device shown in Figure 2 is a diode. The circuit equation for a diode is

$$I_d = I_0(e^{qV_d/KT} - 1) \tag{2}$$

where '$I_d$' is the diode current, '$I_0$' the saturation current, '$q$' the charge of an electron, '$K$' is Boltzmann's constant, and '$T$' the temperature of the diode. At any given time step, first the terminal voltage of the diode is calculated by integrating the component of the electric field along a line from the position of one physical lead to the other, $V = \int_L \bar{E} \cdot \overline{dL}$. The path is from the positive terminal to the negative as indicated in Figure 2. The resulting voltage is used in equation (2) to obtain the device current. Finally, the diode current source is implemented in the FDTD grid by explicitly setting the magnetic fields along a contour, C, which completely encloses one of the conductors attached to the diode. The fields are set in the right-hand sense indicated by the arrows placed on the contour, C, shown in Figure 2. The magnitude of the magnetic fields are determined by the magnitude of the calculated current and the length of the contour according to a static field approximation. Therefore, $H = I_d/L_C$, where $L_C$ is the total length of the contour, and $I_d$ the current through the diode.

## 3. Application to modelling a MESFET

The application of the equivalent source method to model a MESFET is developed based on a general model of a transistor and the Curtice–Cubic model. The transistor update equations are incorporated into a regular FDTD grid by representing the transistor as a two port device as shown in Figure 3. The gate current, $I_g$, and the drain current, $I_d$, flowing into the device are

 

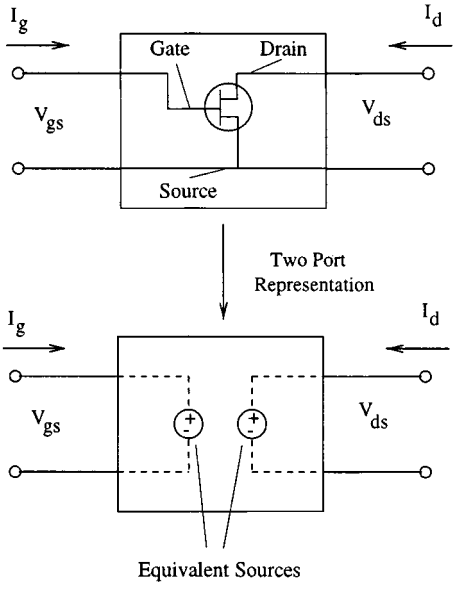


Figure 3. Two port representation of the transistor

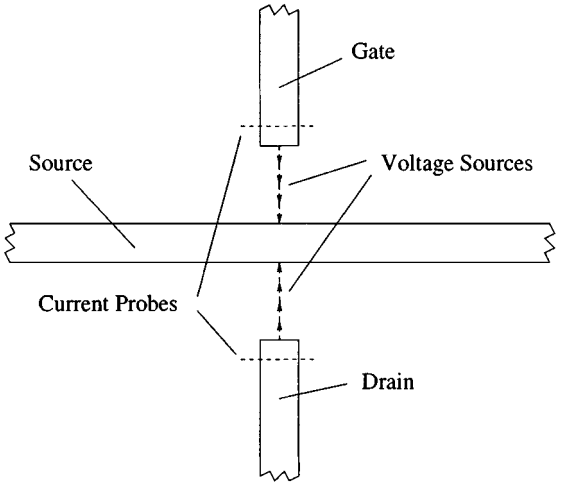


Figure 4. Typical implementation of the transistor across three conductors

calculated using separate line integrals of the form, $\oint H \cdot \mathrm{d}l = I$. Each integral is evaluated along a path which encloses one of the conductors connected to the port of interest. After the normal magnetic field update is performed, the gate to source voltage, $V_{\mathrm{gs}}$, and the drain to source voltage, $V_{\mathrm{ds}}$, are calculated using $I_{\mathrm{g}}$ and $I_{\mathrm{d}}$ in the Curtice–Cubic equations. Finally, the port voltages, $V_{\mathrm{gs}}$ and $V_{\mathrm{ds}}$, are returned to the FDTD grid by setting the electric fields uniformly in the direction of the device according to $E = V_{\mathrm{port}}/L$, where $L$ is the physical length that the port spans. Figure 4 is a depiction of the implementation of the transistor in a FDTD grid.

 

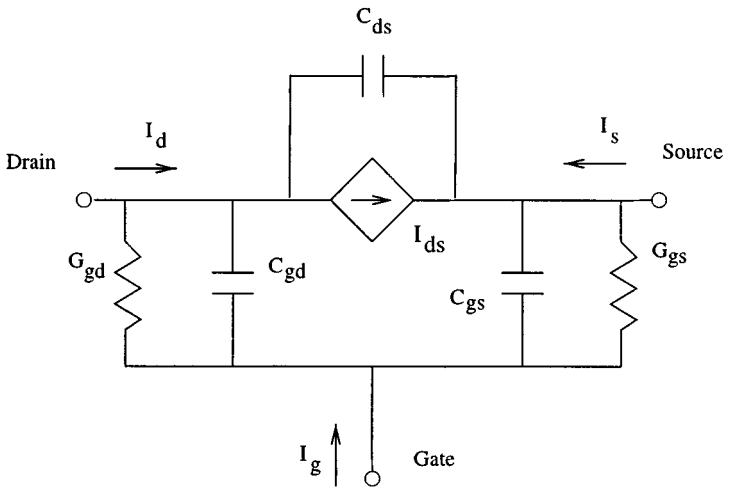


Figure 5. General MESFET equivalent circuit

The circuit equations for the transistor are developed by first analysing a general transistor model and then by applying the Curtice–Cubic model to $I_{ds}$. In the following derivation, the notation for capacitances, conductances, currents, and voltages are denoted by uppercase $C$'s, $G$'s, $I$'s, and $V$'s, respectively. Subscripts indicate the reference of each parameter, where 'g' stands for the gate, 'd' stands for the drain, and 's' stands for the source. For example, $C_{gs}$, is the gate to source capacitance. Furthermore, the time derivative of a specific quantity is denoted by a dot above the quantity, e.g. $\dot{V}_{gs}$, and when applicable, a superscript will indicate the time-step. For example, $V^n_{gs}$, is the gate to source voltage at time step $n$.

Consider the generalized circuit model of a MESFET shown in Figure 5. Applying Kirchhoff's current law to the drain, gate, and source nodes of the equivalent circuit yields:

$$I_d = I_{ds} + \dot{V}_{ds}C_{ds} - V_{gd}G_{gd} - \dot{V}_{gd}C_{gd} \tag{3}$$

$$I_g = \dot{V}_{gd}C_{gd} + V_{gd}G_{gd} + V_{gs}G_{gs} + \dot{V}_{gs}C_{gs} \tag{4}$$

$$I_s = -V_{gs}G_{gs} - \dot{V}_{gs}C_{gs} - I_{ds} - \dot{V}_{ds}C_{ds} \tag{5}$$

In addition, if the gate to drain port voltage is written in terms of the drain to source and the gate to source voltages,

$$V_{gd} = V_{gs} - V_{ds} \tag{6}$$

then only two of the equations (3)–(5) are required for the solution of the system. Arbitrarily choosing equations (3) and (4), and using the relation in equation (6), the system may be rewritten as two equations in terms of the two-port voltages and currents as shown below:

$$(C_{gd} + C_{ds})\dot{V}_{ds} - C_{gd}\dot{V}_{gs} = I_d - I_{ds} + G_{gd}(V_{gs} - V_{ds}) \tag{7}$$

$$-C_{gd}\dot{V}_{ds} + (C_{gd} + C_{gs})\dot{V}_{gs} = I_g - G_{gd}(V_{gs} - V_{ds}) - G_{gs}V_{gs} \tag{8}$$

 

Finally, taking a time derivative of the system of equations, applying finite-differences to the derivatives, and solving for the unknown voltage quantities gives the updates for the gate to source and the drain to source voltages:

$$V_{\mathrm{gs}}^{n+1} = V_{\mathrm{gs}}^{n} + \frac{\Delta t}{\Psi}\left[C_{\mathrm{gd}}(I_{\mathrm{d}}^{n} - I_{\mathrm{ds}}^{n}) + (C_{\mathrm{gd}} + C_{\mathrm{ds}})I_{\mathrm{g}}^{n} + C_{\mathrm{ds}}C_{\mathrm{gd}}V_{\mathrm{ds}}^{n} - (C_{\mathrm{ds}}G_{\mathrm{gd}} + G_{\mathrm{gs}}C_{\mathrm{gd}} + G_{\mathrm{gs}}C_{\mathrm{ds}})V_{\mathrm{gs}}^{n}\right] \tag{9}$$

$$V_{\mathrm{ds}}^{n+1} = V_{\mathrm{ds}}^{n} + \frac{\Delta t}{\Psi}\left[(C_{\mathrm{gd}} + C_{\mathrm{gs}})(I_{\mathrm{d}}^{n} - I_{\mathrm{ds}}^{n}) + C_{\mathrm{gd}}I_{\mathrm{g}}^{n} - G_{\mathrm{gd}}C_{\mathrm{gs}}V_{\mathrm{ds}}^{n} + (C_{\mathrm{gs}}G_{\mathrm{gd}} - G_{\mathrm{gs}}C_{\mathrm{gd}})V_{\mathrm{gs}}^{n}\right] \tag{10}$$

where $\Psi = (C_{\mathrm{ds}}C_{\mathrm{gd}} + C_{\mathrm{gs}}C_{\mathrm{gd}} + C_{\mathrm{ds}}C_{\mathrm{gs}})$. These are the update equations for the general transistor model. These updates are used to find the port voltages of the transistor based on the input currents from the FDTD grid.

The Curtice–Cubic model for a MESFET is given by introducing the following relations for the elements of the general model:[8–10]

$$I_{\mathrm{ds}} = (A_0 + A_1V_1 + A_2V_1^2 + A_3V_1^3)\tanh(\gamma V_{\mathrm{ds}}) \tag{11}$$

The drain to source current, $I_{\mathrm{ds}}$, is a cubic equation of the input voltage, $V_1$. The coefficients, $A_0 - A_3$, are variables that are specified for a specific series of transistor, such as the NEC 71000 series used in the example presented below. The transistor drain current is also governed by a hyperbolic relation of $V_{\mathrm{ds}}$ multiplied by the hyperbolic tangent function parameter, $\gamma$, which is another factor dependent on the particular transistor series. The input voltage is given by the following relation:

$$V_1 = V_{\mathrm{gs}}\{1 + \beta(V_{\mathrm{ds0}} - V_{\mathrm{ds}})\} \tag{12}$$

where $V_{\mathrm{ds0}}$ is the value of $V_{\mathrm{ds}}$ at which $A_0$–$A_3$ were found, and $\beta$ is the coefficient for pinchoff change with $V_{\mathrm{ds}}$. In addition to the non-linear drain to source current, the semiconductor–metal junctions of MESFETs have non-linear capacitances. In fact, the junction capacitance, $C_{\mathrm{d}}$, increases from its nominal value at DC, $C_{\mathrm{d0}}$, with the applied voltage across the junction, $V_{\mathrm{applied}}$, by the following relation:

$$C_{\mathrm{d}} = C_{\mathrm{d0}}\left(1 - \frac{V_{\mathrm{applied}}}{V_{\mathrm{bi}}}\right)^{-\frac{1}{2}} \tag{13}$$

where $V_{\mathrm{applied}}$ is the voltage across the junction and $V_{\mathrm{bi}}$ is the junction's built in voltage. Equation (13) may be used to model both the drain to gate capacitance and the gate to source capacitance.

The pn junctions of the transistor are modelled by a non-linear conductance at each junction. These are the gate to drain conductance, $G_{\mathrm{gd}}$, and the gate to source conductance, $G_{\mathrm{gs}}$. The equation for the conductances is given below:

$$G_{\mathrm{d}} = \frac{I_{\mathrm{s}}}{V_{\mathrm{d}}}(\mathrm{e}^{V_{\mathrm{d}}/V_{\mathrm{t}}} - 1) \tag{14}$$

where $G_{\mathrm{d}}$ is the junction conductance, $I_{\mathrm{s}}$ is the saturation current, $V_{\mathrm{d}}$ is the voltage across the junction, and $V_{\mathrm{t}}$ is the threshold voltage.

 

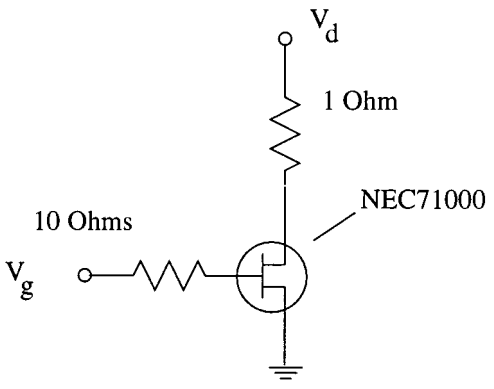


Figure 6. Biasing configuration for transistor equations

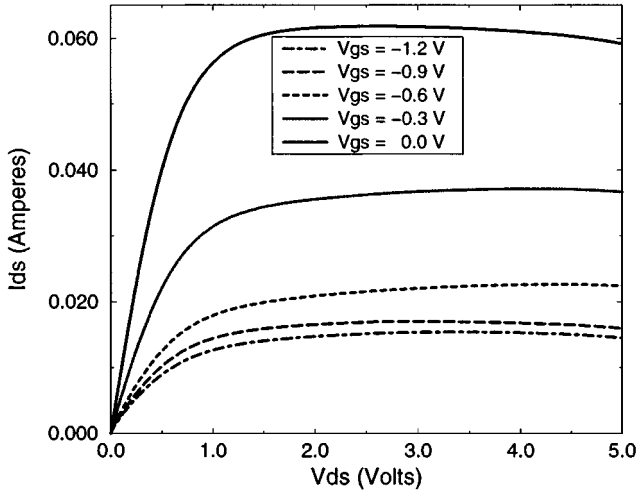


Figure 7. DC curves calculated from transistor equations

The update equations for the transistor given by (9) and (10) with the Curtice–Cubic relations are implemented in a biasing configuration shown in Figure 6 in order to ensure that the non-linear behaviour of the transistor was being properly modelled.

The FDTD results of biasing simulations for several values of $V_{gs}$ are presented in Figure 7. These curves display the non-linear behaviour of the transistor model. The same biasing configuration is used in MDS simulations for comparison and are presented in Figure 8. MDS is a frequency domain circuit simulator based on lumped element and transmission line equations and it employs its own proprietary algorithms to the Curtice–Cubic model. It is evident that the characteristics of the two models are similar, however, the MDS model exhibits cutoff for smaller magnitudes of $V_{gs}$ than the FDTD model.

 

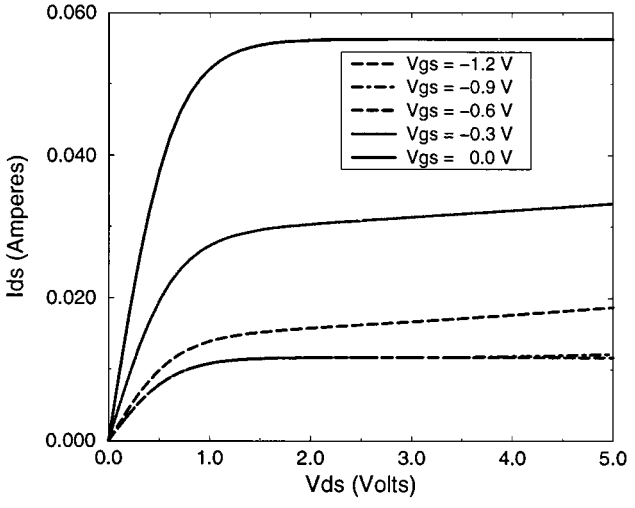


Figure 8. MESFET DC curves from MDS simulation

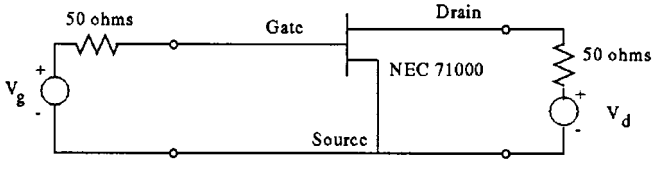


Figure 9. FDTD circuit model used to extract s-parameters

## 4. Initial results

By using the updates given in equations (9) and (10) in a common source circuit is shown in Figure 9, the s-parameters of the FDTD Curtice–Cubic model can be calculated. The model was based on the NEC 71000 MESFET with the parameters of the Curtice–Cubic model being provided by the manufacturer.[11] It is important to note that the electric and magnetic field updates were not used for calculation of the s-parameters. Only the FDTD equations for the resistors, sources, and the transistor using the Curtice–Cubic model were used. Since the s-parameters depend on the operating point of the transistor, the transistor must be biased to a common operating point between the simulations and the manufacturer's measured data for a proper comparison. The operating point specified by the manufacturer was $V_{ds} = 3{\cdot}0$ V and drain current of 30 mA. To obtain the proper $V_{ds}$ and $I_d$, the sources, $V_g$ and $V_d$ must be ramped up at a rate slow enough to retain numerical stability. The exact rate above which the simulation becomes numerically unstable for a given time step value is difficult to derive for complex, non-linear models such as this, however, it was found that the stability conditions that the normal FDTD grids enforce on the time step was usually more stringent than the MESFET model required. The transitions of the two-port voltages to the proper bias point are shown in Figure 10. First, the gate-to-source voltage is negatively biased to put the transistor in the cutoff region.

 

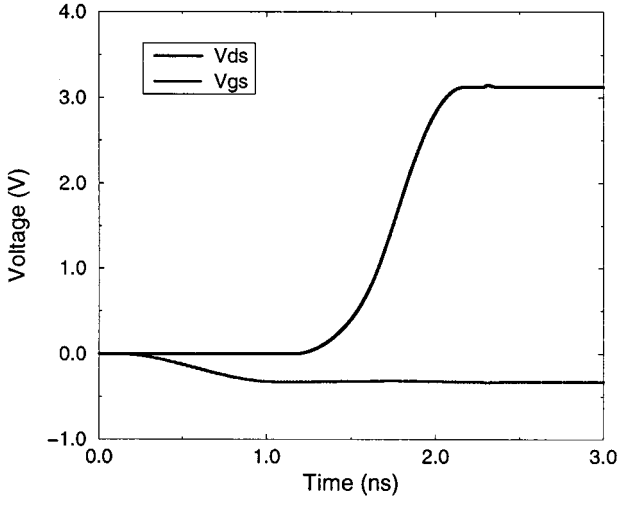


Figure 10. Bias voltage curves with small incident Gaussian pulse imposed on vgs

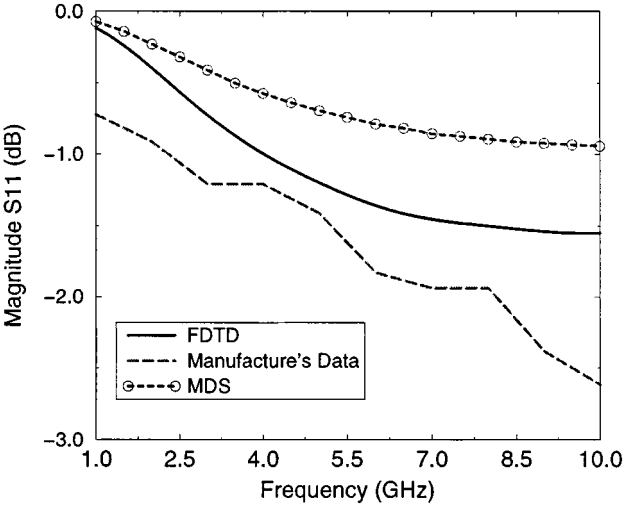


Figure 11. Comparison of FDTD, MDS, and manufacturer's S11 with frequency

Next, the drain-to-source voltage is biased up to 3 V. After the voltages have settled, an incident Gaussian pulse with an amplitude of 0·02 V is superimposed on $V_{gs}$ as an input signal. The small amplitude is required to obtain the small signal s-parameters. The incident pulse and the total voltages of the input ($V_{gs}$) and output ($V_{ds}$) are recorded, time gated, and separated from the bias voltages. Finally a discrete Fourier transform is applied to these values to find S11 and S12. To obtain S21 and S22, the incident Gaussian is imposed on the drain-to-source voltage as the input signal to port 2 and the process is repeated.

 

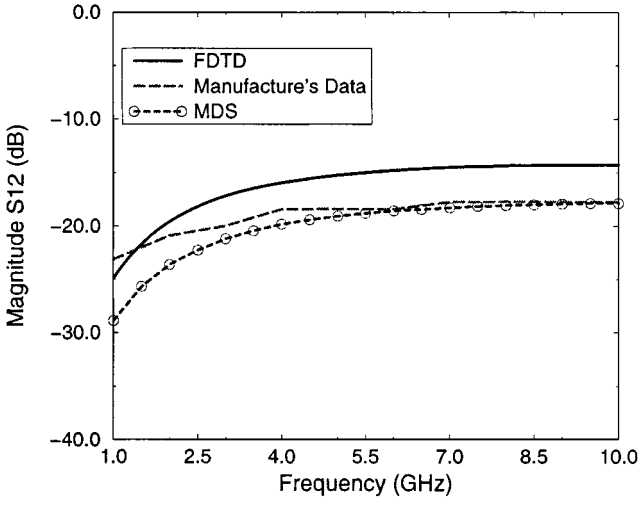


Figure 12. Comparison of FDTD, MDS, and manufacturer's S12 with frequency

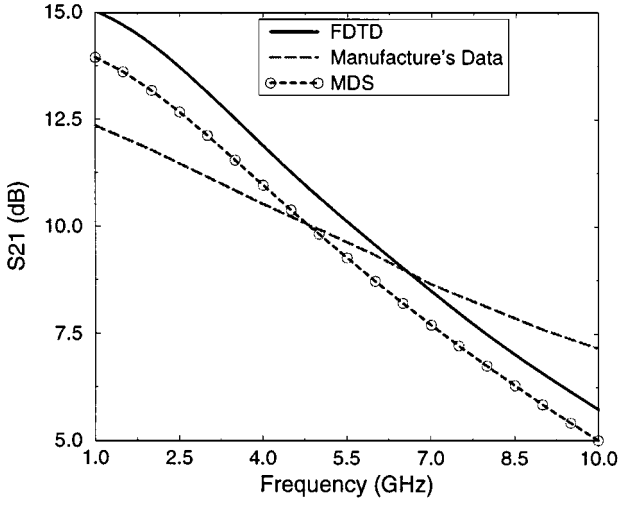


Figure 13. Comparison of FDTD, MDS, and manufacturer's S21 with frequency

For comparison, MDS was used to perform s-parameter simulations of the Curtice–Cubic model. The FDTD and MDS results are presented in Figures 11–14 along with the measured data provided by the manufacturer.

Excluding S22, the two simulation models give the same trends and are relatively close. The manufacture's measured data is based on network analyzer measurements that include inductances due to the bond wires that connect the transistor IC to the test fixture. Both the MDS and the FDTD models neglect this bond wire inductance, which may explain some of the discrepancy between the measured and modelled results.

 

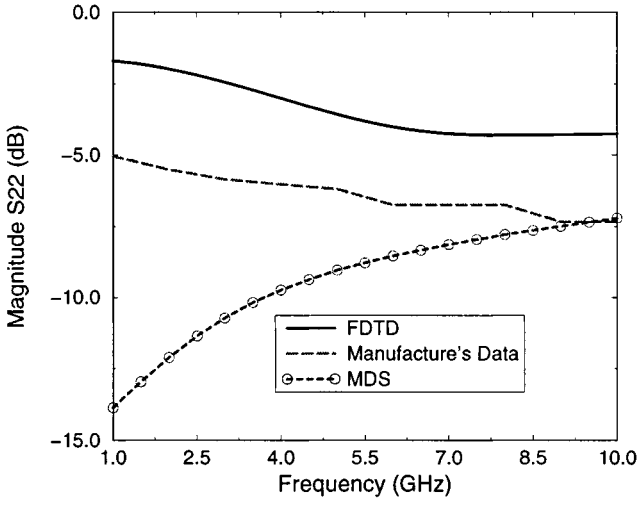


Figure 14. Comparison of FDTD, MDS, and manufacturer's S22 with frequency

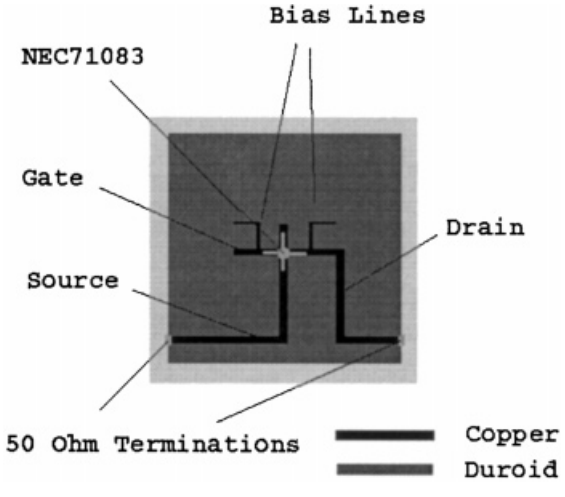


Figure 15. Diagram of the experimental circuit layout

## 5. Three port oscillator

A typical application that requires a non-linear transistor model is an oscillator. A three-port transistor oscillator may be constructed by connecting a resonant length of open circuited transmission line to the gate terminal of the transistor and terminating the source and drain terminals with 50 Ω resistors. A diagram of a three-port oscillator circuit is shown in Figure 15.

The circuit is built on 20 mil thick Duroid with a 2·2 relative permittivity and the uses a NEC 71083 transistor. The length of the open circuited line connected to the gate terminal is

 

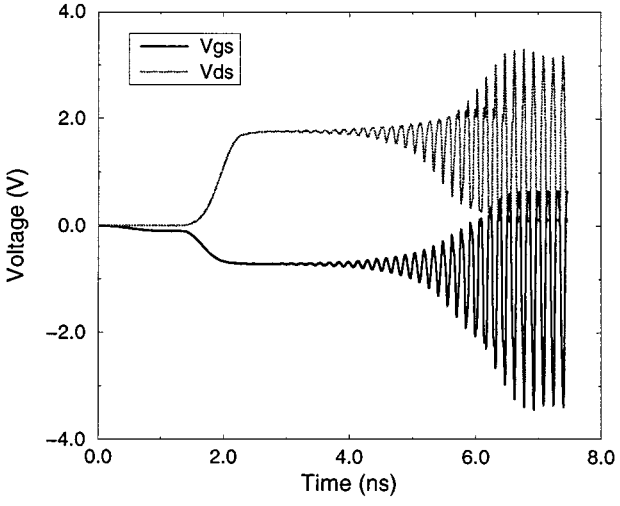


Figure 16. Transient voltage curves for the three port oscillator showing onset of oscillation

9·1 mm – designed to produce a 5·0 GHz oscillation frequency. The simulation grid is a regular mesh of $30 \times 60 \times 80$ FDTD cells that are 0·5 mm on a side. The split-field perfectly matched layer (PML) absorbing boundary condition is used on all sides of the FDTD grid.[12–14] The PML is second order, six cells deep, and its maximum theoretical reflection coefficient at normal incidence is specified to be $R_{\max} = 1 \times 10^{-6}$. The FDTD model includes non-linear capacitances for both the gate to source and the drain to gate junctions. The transient drain to source and gate to source voltages from the FDTD simulation are shown in Figure 16. This displays the biasing of the transister and the onset of oscillation. The frequency spectrum of the oscillator can be found by taking Fourier transform of the gate current. The results of the transform indicates a fundamental oscillation frequency of 6·0 GHz for the FDTD model. Measurements of the frequency spectrum of the oscillator using a spectrum analyser indicates that the physical circuit oscillates at 50·46 GHz. This is roughly a 10% relative error between FDTD and experimental results. The most likely the cause for the discrepancy between the predicted and the experimental results is that the FDTD model does not include package parasitics, however, further investigation will be performed.

## 6. Conclusions

A new approach to modelling 3D lumped elements in a finite-difference time-domain grid is presented. The equations for a general transistor model are derived and then finite-differences are applied to obtain update equations for the transistor voltages. These update equations are then implemented in a FDTD grid using a two port representation for the transistor and a Curtice–Cubic model for the transistor characteristics. This technique is then applied to a simple common source circuit and a comparison of the extracted s-parameters is made between the FDTD model, the manufacture's measured data, and a similar MDS Curtice–Cubic model. Next, the transistor model is implemented in a FDTD grid using a three port oscillator configuration. The start-up transients and the onset of oscillation are observed from the

 

simulation and the simulation's oscillation frequency is compared to measurements performed on a physical circuit. The advantages provided by this method over the extended FDTD method is the elimination of a separate non-linear technique required to solve the transcendental equations resulting from the extended formulation. The separate non-linear solver must be employed at every time step in the extended FDTD method. Therefore, the equivalent source method provides a savings in computational cost over the extended FDTD method. The extended FDTD method also produces complex field updates that require matrix solutions when the lumped element spans more than one cell. These matrices increase in size as the square of the number of cells spanned by the lumped element. The equivalent source method allows the lumped element to be easily extended across multiple cells without a significant modification to the method and without an increase in computational cost.

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