Efficiency of Chip-Level Versus External Power Combining

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***Abstract*— In this paper, we compare two X-band high-efficiency switched-mode amplifiers designed around two commercially available packaged MESFET's, one having a four times larger gate periphery than the other. The amplifiers using the larger and smaller devices are designed to operate in classes E and F, respectively. The smaller device gives 685-mW output power with 7.4-dB gain and 64% overall efficiency. The larger device gives 1.70-W output power with 5.3-dB gain and 57% overall efficiency. This gives an internal (or chip-level) power-combining efficiency for the larger device of 89% in terms of *overall efficiency*. This is compared to the combining efficiency of circuit and spatial power combining using high-efficiency amplifiers, with the goal of assessing which architecture is the most efficient in terms of total dissipated power (dc and RF).**

***Index Terms*— Power amplifiers, power combining, high efficiency.**

I. Introduction

INCREASED commercial use of the millimeter-wave spectrum has created an urgent need for medium- to high-power millimeter-wave sources. This need has traditionally been met by vacuum devices such as klystrons and traveling-wave tubes. Rapid advances in high-frequency semiconductor-device technology has made it possible to replace vacuum devices with lighter and less expensive solid-state devices that do not require high-voltage power supplies. However, due to the limited output power from millimeter-wave semiconductor devices, the outputs of tens or even hundreds of devices must be combined.

For a large number of applications, e.g., base-station transmitters in communication, tens of watts of microwave power are required. The dc power consumption can be greatly reduced by increasing the amplifier efficiency. However, the efficiency becomes lower as device size increases, thus, combining smaller amplifiers to achieve these power levels is an attractive option. The goal of this paper is to compare several amplifier architectures with optimization of power consumption in mind and to define a power-combining efficiency (PCE) useful for that purpose.

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There are two basic methods of power combining: internal (or chip-level) and external. The latter includes methods such as circuit corporate and spatial power combiners. At the device level, the gate periphery can be enlarged to increase the power potential of the individual device at the expense of gain and efficiency. Alternatively, smaller and more efficient amplifiers can be combined externally (off-chip). Both internal and external power combining can be used together. For instance, ten 1-mm MESFET's can be circuit combined instead of 20 0.5-mm devices for the same output power.

The Fujitsu FLK052WG MESFET and the Fujitsu FLK202MH-14 are used in this paper for a comparison. The FLK052 and the FLK202 have the same intrinsic structure, but the periphery of the FLK202 is four times larger [1]. They are both packaged devices.

II. Chip-Level Power Combining

Considering that the FLK202 is physically four times larger than the FLK052, the output power might be expected to be four times larger as well. The goal in low-power electronics, however, is to minimize power dissipation. It is, therefore, more relevant to define the chip-level PCE $(\mathrm{PCE_{chip}})$ as the ratio of the *overall efficiency* of the FLK202 amplifier to the FLK052 amplifier

$$\mathrm{PCE_{chip}} = \frac{\eta_{\mathrm{AMP},202}}{\eta_{\mathrm{AMP},052}} \tag{1}$$

where η_{AMP} is the overall efficiency given by

$$\eta_{\mathrm{AMP}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{DC}} + P_{\mathrm{in}}}. \tag{2}$$

In order to accurately calculate $\mathrm{PCE_{chip}}$ for the FLK202 MESFET, both devices should be used in a power amplifier that yields the highest possible efficiency at a given frequency and bias point. It was found experimentally that, around 8 GHz, the FLK052 gave the best overall efficiency in a class-F amplifier and the FLK202 gave the best overall efficiency in a class-E amplifier, while maintaining high output power.

A. Power-Amplifier Design

A switched-mode class-F amplifier using the FLK052 was designed on a 0.508-mm Rogers Duroid RT5880 $(\epsilon_r = 2.2)$. The fundamental is terminated in the impedance for maximum saturated power delivered to the load. This impedance is given

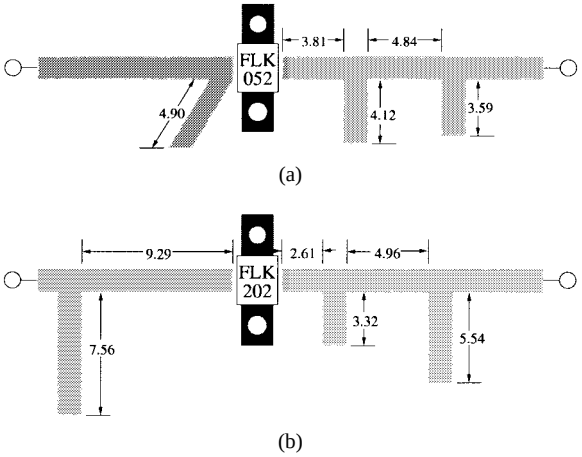

Fig. 1. Microstrip layout of: (a) the class-F amplifier using the FLK052 and (b) the class-E amplifier using the FLK202. The substrate is 0.508-mm-thick RT5880 Duroid ($\epsilon_r = 2.2$). All dimensions are given in millimeters.

approximately by [2]

$$Z_{\text{net}} = \frac{2V_{\text{DS}}}{I_{\text{DSS}}}$$

where I_{DSS} is the maximum saturated drain current. The drain capacitance and drain lead inductance of the MESFET are deembedded and included in the external tuned circuit. The second harmonic is terminated in a short. The layout of the amplifier is shown in Fig. 1(a). The 3.81-mm line and 4.12-mm open stub provide the second harmonic short. This in combination with the 4.84-mm line and the 3.59-mm open stub provide the fundamental match.

Using the FLK202, a class-E amplifier was designed on the same substrate. The microstrip layout is shown in Fig. 1(b). The class-E amplifier is a resonant switched-mode circuit in which a switch turns on at zero voltage and zero derivative of voltage. Ideally, the product of the switch voltage and current is zero, resulting in 100% efficiency. At microwave frequencies, however, an ideal switch is not available. In a microwave class-E amplifier, a MESFET is driven as a switch. It can be shown [3] that the output impedance for ideal class-E operation is given by

$$Z_{\text{net}} = \frac{0.280\,15}{\omega_s C_s} e^{j49.0524^\circ} \tag{3}$$

where $\omega_s/2\pi$ is the fundamental or desired harmonic and C_s is the switch output capacitance, approximated by C_{ds}. The second harmonic is terminated in an open circuit, provided by the 2.61-mm line and 3.32-mm stub. The 4.96-mm line and 5.54-mm stub in combination with the second harmonic circuitry provide the class-E impedance at the fundamental.

B. Power-Amplifier Measurements

The output power and efficiency for each amplifier were measured as a function of frequency and input power. Fig. 2 shows the output power and overall efficiency versus frequency for the FLK052 class-F and the FLK202 class-E amplifiers. Fig. 3 shows the output power and overall efficiency versus input power for the FLK052 amplifier and the FLK202 amplifier. Table I shows the best performance of each amplifier. The FLK052 class-F amplifier has a high η_{AMP} at 8.4 GHz of 64% with 685-mW output power. The FLK202 class-E amplifier has a high η_{AMP} at 8.35 GHz of 57% with 1.7-W output power. From (1), the chip-level PCE of the FLK202 is 89%.

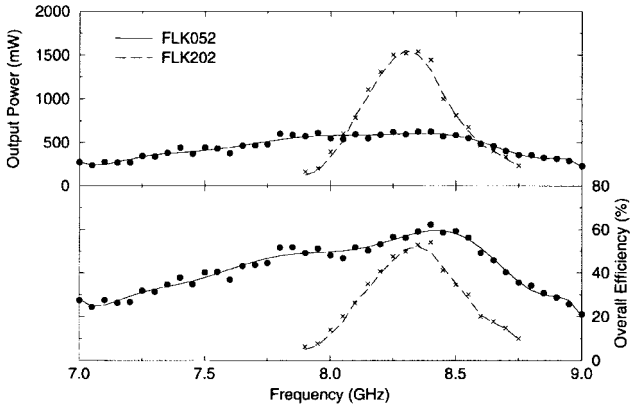

Fig. 2. Output power and overall efficiency versus frequency for the FLK052 class-F amplifier (solid line) and the FLK202 class-E amplifier (dashed line). The input power is 20 dBm for the FLK052 class-F amplifier and 26 dBm for the FLK202 class-E amplifier. $V_{\text{DS}} = 7.0$ V and $V_{\text{GS}} = -0.9$ V.

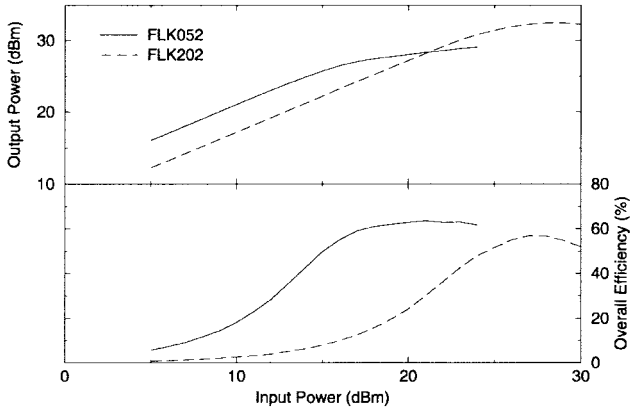

Fig. 3. Output power and overall efficiency versus input power for the FLK052 class-F amplifier (solid line) and the FLK202 class-E amplifier (dashed line). The frequency is 8.4 GHz for the FLK052 amplifier and 8.35 GHz for the FLK202 amplifier. $V_{\text{DS}} = 7.0$ V and $V_{\text{GS}} = -0.9$ V.

TABLE I
SUMMARY OF MEASUREMENTS FOR THE CLASS-F POWER AMPLIFIER USING THE FLK052 AND THE CLASS-E POWER AMPLIFIER USING THE FOUR-TIMES LARGER FLK202. P_{heat} IS THE POWER DISSIPATED AS HEAT

Device	P_{in}	P_{out}	Gain	η_{AMP}	P_{heat}
FLK202	500 mW	1.700 W	5.3 dB	57%	1.300 W
FLK052	125 mW	685 mW	7.4 dB	64%	391 mW

III. CIRCUIT-LEVEL POWER COMBINING

In a circuit corporate combiner, shown in Fig. 4, the outputs from each amplifier are successively combined using two-way adders, such as Wilkinson combiners. Table II shows a comparison, for the same input power, between the circuit corporate combining of four FLK202 amplifiers and 16 FLK052

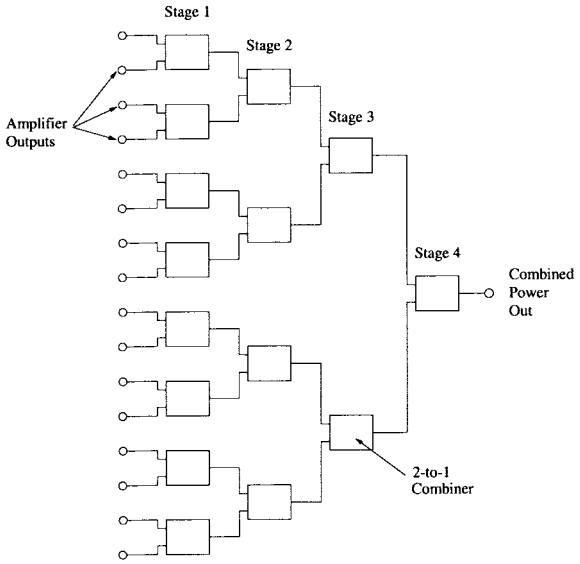

Fig. 4. A circuit corporate power combiner. The output of an amplifier is connected to each circle.

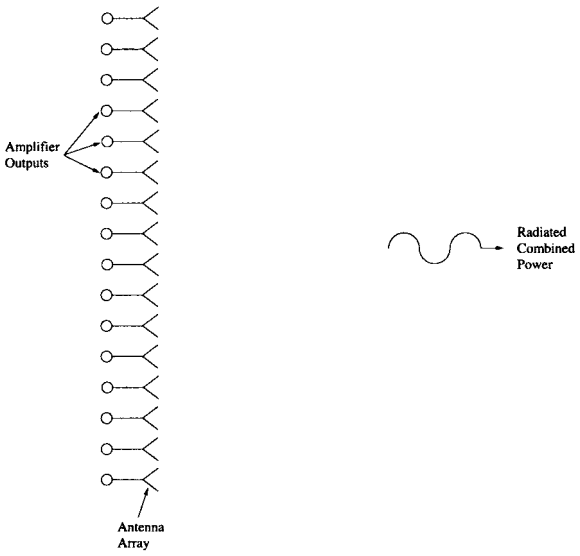

Fig. 5. Spatial power combiner. The output of an amplifier is connected to each circle.

TABLE II
COMPARISON OF [FOR THE SAME INPUT POWER (8 W)] CHIP-LEVELCOMBINING VERSUS CIRCUIT COMBINING FOR A CORPORATE COMBINER WITH 0.2-dB LOSS PER STAGE. η_{AMP} IS THE OVERALL EFFICIENCY OF THE AMPLIFIER, $\mathrm{PCE_{ckt}}$ IS THE POWER-COMBINING EFFICIENCY OF THE CORPORATE NETWORK, AND η IS THE OVERALL EFFICIENCY OF THE ENTIRE SYSTEM. P_{heat} IS THE TOTAL POWER DISSIPATED AS HEAT IN THE SYSTEM

Device	N	η_{AMP}	Stages	$\mathrm{PCE_{ckt}}$	$\mathrm{P_{out}}$	η	$\mathrm{P_{heat}}$
FLK202	16	57%	4	83%	22.6 W	47%	25.5 W
FLK052	64	64%	6	76%	33.3 W	49%	34.7 W

amplifiers for 0.2-dB loss per stage. To find the overall efficiency of the entire system (η), the overall efficiency of the amplifier (η_{AMP}) is multiplied by the PCE of the combining network $(\mathrm{PCE_{ckt}})$ given by

$$\mathrm{PCE_{ckt}} = 10^{-n\frac{\mathrm{L}}{10}} \tag{4}$$

where L is the loss per stage in decibels and n is the number of stages. The total number of elements N is 2^n. Even for a low-loss combiner (0.2-dB loss), the overall efficiencies are approximately equal, but it would be less complex and use less space to combine the four larger FLK202 amplifiers.

IV. SPATIAL POWER COMBINING

Spatial, or *quasi-optical*, power combining, shown in Fig. 5, eliminates the need for complicated and lossy corporate networks. In this approach, the output of each amplifier is connected to an antenna. The powers from all the devices are thus coherently combined in free space in a single stage. The PCE is, therefore, independent of the number of elements. This approach was first demonstrated in 1968 with a 100-element array at 410 MHz [4]. Other examples include a two-stage 14-element X-band lens array with 75% PCE [5] and a four-element 5-GHz class-E array with 64% power-added efficiency and an estimated PCE of about 80% [3]. A survey of spatial power-combining techniques can be found in [6].

Table III shows a comparison between spatially combining four FLK202 amplifiers and 16 FLK052 amplifiers. The overall efficiency of the entire system is η_{AMP} times the PCE of the spatial combiner $(\mathrm{PCE_{spc}})$. A value of 75% is assumed for $\mathrm{PCE_{spc}}$. This includes the efficiency of the antennas. P_{out} is equal to the output power from each amplifier multiplied by $N \cdot \mathrm{PCE_{spc}}$. The area of the combining array assumes a unit cell size of $0.8\lambda \times 0.8\lambda$ and is, therefore, equal to $0.64 \cdot N\lambda^2$. The directivity D assumes an effective area equal to the physical area and is, therefore, equal to $4\pi/\lambda^2 \cdot \mathrm{Area}$. The effective isotropic radiated power (EIRP) is the directivity multiplied by P_{out}.

Since the PCE is independent of the number of elements, it is more efficient in a spatial combiner to use a larger number of smaller amplifiers if space is not an issue. In addition, a larger array has a higher directivity, thus, the EIRP is also higher. Thermal management also becomes easier if a larger numbers of smaller devices are used since the heat flux is much less.

In order to compare circuit to spatial combining, an antenna should be placed at the output of the circuit combiner. Assuming that the choice of antenna is not constrained by size or substrate considerations, unlike the spatial combiner, this antenna can be close to 100% efficient. A comparison of circuit combining to spatial combining shows that for 0.2-dB loss per stage, a circuit combiner with more than six stages (64 elements) will have a lower PCE than the 75%-efficient spatial combiner.

Since output power-combining efficiencies are being compared, the input power distribution (feed) network has not been mentioned. A spatial power combiner can either be circuit fed, using a corporate structure similar to Fig. 4 as a divider, or spatially fed, where the feed is also in free space. The circuit-fed approach has the same problems with loss as a circuit combiner, but amplifiers can be placed in the input network to account for this. The spatially fed approach has two problems:

TABLE III
COMPARISON OF [FOR THE SAME INPUT POWER (8 W)] THE SPATIAL POWER COMBINING OF 16 FLK202 AMPLIFIERS AND 64 FLK052 AMPLIFIERS. THE AREA ASSUMES A UNIT CELL SIZE OF $0.8\lambda \times 0.8\lambda$. THE DIRECTIVITY D ASSUMES AN EFFECTIVE AREA EQUAL TO THE PHYSICAL AREA. P_{heat} IS THE TOTAL POWER DISSIPATED AS HEAT IN THE SYSTEM

Device	N	η_{AMP}	P_{out}	η	P_{heat}	Area	Heat Flux	D	EIRP
FLK202	16	57%	20.4 W	43%	27.0 W	131 cm^2	207 $\frac{\mathrm{mW}}{\mathrm{cm}^2}$	21.1 dB	2.63 kW
FLK052	64	64%	32.9 W	48%	35.6 W	522.4 cm^2	68 $\frac{\mathrm{mW}}{\mathrm{cm}^2}$	27.1 dB	16.9 kW

spillover loss and amplitude and phase nonuniformities. As with the circuit-fed approach, spillover loss results in the need of extra amplification at the input. Phase nonuniformities can be eliminated by using a constrained lens approach [7] or by using an external lens to generate a Gaussian beam [8]. Amplitude nonuniformities can cause problems if the effects of phase compression are not accounted for. A thorough comparison between circuit- and spatial-fed combiners can be found in [9].

V. CONCLUSION

In summary, high-efficiency power amplifiers were designed using MESFET's with identical intrinsic structure, but different gate peripheries. Also, a new definition of PCE is given, which is applicable to the problem of minimizing power dissipation. Measurements indicate, for the larger device, a chip-level PCE of 89% in terms of overall efficiency. However, this approach is limited by propagation delays as the device periphery increases. Also, the input impedance drops as the number of gate fingers increases, reducing bandwidth.

Using these power amplifiers, an overall efficiency was calculated for circuit and spatial combiners. In circuit combiners, a small number of larger devices was found to be more efficient. In spatial combiners, it is more efficient to use a large number of smaller devices. In addition, in applications which require an antenna array at the transmitter output, distributed amplification (spatial combining) has advantages with respect to EIRP and thermal management.

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