An X/K-band Class-E High-Efficiency Frequency Doubler

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***Abstract*—**

A class-E frequency doubler is presented at 20.8 GHz, the highest frequency reported to date. The circuit has 42.7% drain efficiency and 31.6% overall efficiency for an output power of 7.1 dBm and 0.83 dB conversion gain. A maximum gain of 7.18 dB is achievable with 3.4 dBm output power and 13.5% overall efficiency. The trade-off between efficiency and conversion gain is optimized by proper biasing and driving to obtain a 5.23 dB gain with an overall efficiency of 23.5%. The rejection of unwanted harmonics is greater than 26 dBm. The MESFET doubler is designed using a simple switching mode theory based on small signal device parameters.

Index terms - Frequency doublers, class-E, high-efficiency.

I. Introduction

In most modern microwave and millimeter-wave communication systems, the signal from a low-frequency, high-quality oscillator is multiplied up to the desired frequency by a chain of frequency multipliers, a general background of which can be found in [1] and [2]. For example, in COMSTAR communication satellites, the signal generated by a high-Q, stable, 9.5 GHz oscillator is multiplied by a diode chain up to 19.04 GHz for use as a beacon [3]. Doubler conversion gains of 4 dB and -1.8 dB are reported at 18 and 20 GHz output frequencies [4] while at a 24 GHz output frequency, -1.9 dB conversion gain was obtained with a drain efficiency of about 5% [5]. The typical output power is about 0-10 dBm.

Frequency multipliers are a primary cause of power dissipation in local oscillator (LO) circuitry, and recent efforts have focused on the design of power-efficient frequency multipiers. For example, low-cost, low-power frequency multipliers with outputs at 762 MHz and 3.050 GHz have been fabricated for mobile wireless applications [6]. High-efficiency class-E frequency multipliers could present a viable method of minimizing heat dissipation near the oscillator as well as lowering power consumption in the LO circuitry. This paper presents a 10.4/20.8 GHz MESFET frequency doubler designed to be highly efficient by operating in class-E mode, in addition to providing conversion gain.

II. Class-E Topology

Class-E power amplifiers have a theoretical DC-RF power conversion efficiency of 100% by operating the transistor as a switch [7]. They have been demonstrated at microwave frequencies upto 10 GHz [8] where a 20 dBm output power was obtained with 74% drain efficiency and 62% power-added efficiency. By proper design of the output tuned circuit of the class-E amplifier, the switch waveforms are shaped such that switching losses are minimized. Further details of class-E amplifier operation are discussed in [9].

Class-E multipliers have been reported at an output frequency of 3.37 MHz and 95% drain efficiency [10], and at 1 GHz and 5 GHz output frequencies with power-added efficiencies of 35% and 29% respectively [11]. The corresponding conversion gains for the last two cases are 8.5 dB and 5.2 dB.

The use of class-E topology at higher frequencies is limited only by device output capacitance, maximum current capability, and drain voltage [12]. For today's commercially available devices this frequency limitation is at about 1-

6 GHz. Above this critical frequency, class-E performance is suboptimal, with a resulting decrease in achievable efficiency. However, even in suboptimal mode, the efficiency of class-E circuits is higher than other classes.

III. Theory of Class-E Multipliers

The design of class-E frequency multipliers has been analyzed by Zulinski and Steadman in [10]. Harmonic generation in a class-E multiplier is due to the switching of the transistor between ON and OFF states by a switching signal of duty cycle D, given by:

$$D = \frac{0.5}{N}, \tag{1}$$

where N is the order of the desired output harmonic. For frequency doubling, the optimum duty cycle is 25%, meaning that the switch voltage is nonzero for 25% of the time. The duty cycle is controlled by the gate bias and RF input power.

By performing a Fourier series analysis on the time domain switch voltage waveform described in [10], the DC drain voltage is found to be:

$$V_{ds} = \frac{I_{max}}{56.5 C_s f N^2}, \tag{2}$$

where f is the switching frequency, and Nf is the output frequency. This means that for the same switching frequency, the drain voltage must decrease as N^2 for an output at a harmonic Nf. This is primarily because the duty cycle decreases with N, while the capacitor-charging slope at $t = 0$ remains the same. This implies a lower peak switch voltage and correspondingly small DC component.

The load impedance required for class-E operation, Z_{load}, is calculated from the ratio of the voltage and current components at the output frequency and is given by:

$$Z_{load}(Nf) = \frac{0.0446}{C_s f N^2} e^{j49.05^\circ}. \tag{3}$$

For the case of the class-E amplifier, this equation is the same as that presented in [12]. For frequency multipliers, the load impedance scales as $1/N^2$. All other harmonics are presented with an open circuit at the output.

IV. Multiplier Design

An AFM04P2 medium power MESFET with 21 dBm output power capability at 18 GHz is used as the switch for a class-E 10/20 GHz frequency doubler based on the equations presented above. The output capacitance, C_{ds}=0.103 pF of the MESFET is extracted from s-parameters. The load impedance at 20 GHz for a switching frequency of 10 GHz is obtained from Eq. (3) to be, $Z_{load} = 7.09 + j8.17\Omega$. This value is then optimized on HP ADS such that the the fundamental rejection is maximized and the output mismatch of the class-E amplifier is minimized such that high conversion gain might be possible. This necessitates a compromise between the ideal class-E match and an ideal output match to 50 Ω. The final value of the 20 GHz load impedance is $Z_{load} = 13.65 + j15.74\Omega$, which maintains the load angle required for class-E operation. The microstrip circuit shown in Fig. 1 was milled on Rogers TMM10 with a dielectric constant of 9.2 and a thickness of 0.381 mm.

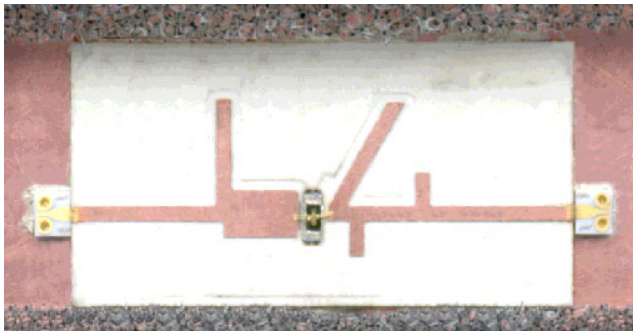


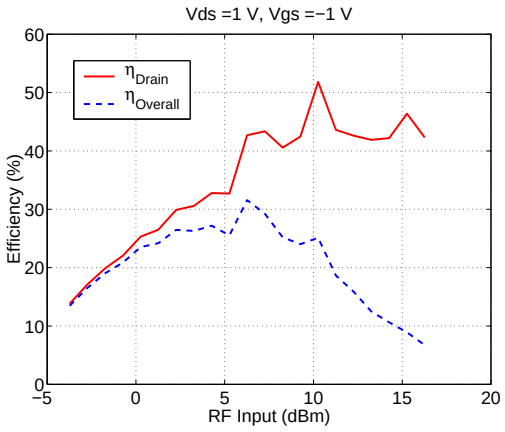
Fig. 1. Photograph of the fabricated 10.4/20.8 GHz multiplier circuit. The 50 Ω transmission lines are 0.4 mm wide.

V. Measurements

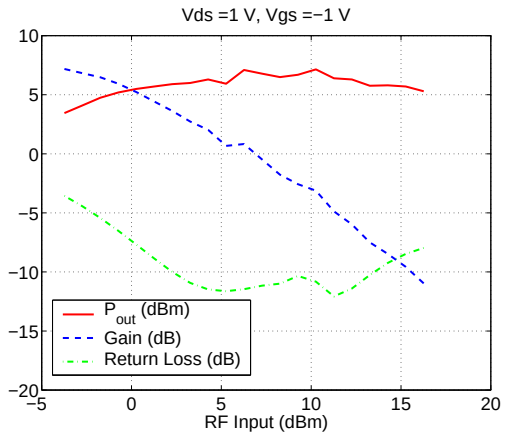
The input match of the doubler was measured at 10.4 GHz and therefore the input frequency to the doubler was set at this value. From small-signal simulations, it was found that the shift in frequency is probably due to a 0.075 mm overetch in the metal transmission lines. An HP70820A Microwave Transition Analyzer was used to measure the doubler power and efficiency performance as a function of input power, drain voltage and gate voltage. Various combinations of gate bias and RF input power were used to obtain different duty cycles whereas different drain bias points are used to verify Eq. (2). The drain voltages used were V_{ds}=0,1,2,..5 V, and the gate voltages were V_{gs}=0,-0.2,-0.7,-1,-1.2, and -1.5 V. The pinch-off voltage of the device is about -1.8 V. At each bias point, the input power was varied from -6 to 17 dBm.

Property	Optimized Property			
	P_{out}, η_D	G	η	G, η
V_{gs} (V)	-0.7	-1	-1	-1
P_{in} (dBm)	9.3	-3.7	6.3	0.3
s_{11} (dB)	-7.4	-3.6	-11.5	-7.7
P_{out}(dBm)	7.5	3.4	7.1	5.5
Gain (dB)	-1.77	7.18	0.83	5.23
η_D (%)	51	13.8	42.7	25.3
η (%)	28.9	13.5	31.6	23.5

Table 1: Optimum Performance of the 10.4/20.8 GHz Doubler. η_D is the drain efficiency and η is the overall efficiency. V_{ds}=1 V.



(a)



(b)

Fig. 2. Measured (a) drain and overall efficiency and (b) output power and conversion gain of the 20.8 GHz doubler as a function of input RF power. The bias point is V_{ds}=1 V, and V_{gs}=-1 V.

A. *Optimum Measured Performance*

The doubler performance can be optimized for drain efficiency, overall efficiency, output power, or conversion gain by proper biasing. Drain efficiency is the DC-RF efficiency given by the ratio of output RF power to input DC power.

In the first column of Table 1, it can be seen that the output power and drain efficiency are maximized simultaneoulsy. 7.5 dBm output power is thus obtained with 51% drain efficiency and 28.9% overall efficiency with a relatively low conversion gain of -1.77 dB. However, as can be seen in column 2 of Table 1, a maximum conversion gain of 7.18 dB with 3.4 dBm output power is achievable with a reduced 13.5% overall efficiency. A reasonably high gain of 5.23 dB can be obtained with moderately high efficiencies of about 25% and about 5.5 dBm output power, as shown in column 4. For optimum overall efficiency, η=30.6%, the gain is lower at 0.83 dB, demonstrating the trade-off between these two quantities, as can be seen in colums 2 and 3 in Table 1.

Fig. 2 shows the performance of the doubler as input RF power is varied. The bias point is V_{ds}=1 V and V_{gs}=-1V for optimum gain and efficiency. Fig. 2(a) a maximum overall efficiency occuring for an input RF power at 10.4 GHz of about 6.3 dBm. The drain efficiency continues increasing with RF input power, but as can be seen from Fig. 2(b), results in decreased conversion gain since the output power remains approximately constant over the range of input power. In addition, the input reflection coefficient varies with bias, affecting the conversion gain of the doubler.

Fig. 3 shows that there is no significant increase in output power as the drain voltage is increased, supporting Eq. (2) which predicts V_{ds} ≈0.6 V. There is a slight increase in output power to about 8 dBm for increased drain voltage, but this comes at the cost of a much lower efficiency, approximately 10%.

B. *Reflection of Harmonic Power Towards The Input*

In order to investigate the harmonic reflection towards the transistor input due to the feedback capacitor C_{gd}, no harmonic tuning was used at the input of the multiplier. In practical multipliers, a shorted or open stub would be used at the input to supress feedback of the harmonic. The reflected second harmonic component was measured at the input to quantify the effects of this feedback capacitor. The reflected power is

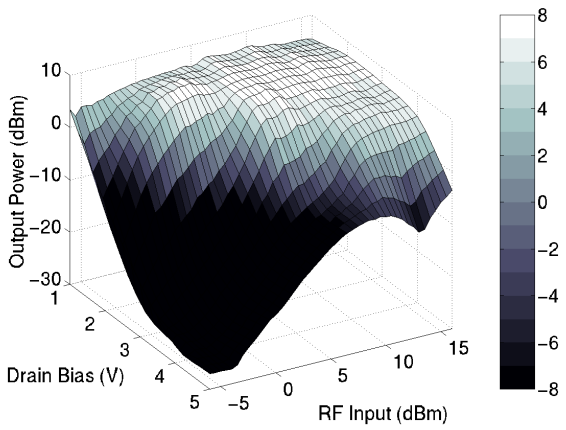


Fig. 3. Measured output power of the 20.8 GHz doubler vs. drain bias and RF input power for V_{gs}=1 V. There is no significant increase in output power as the drain voltage is increased.

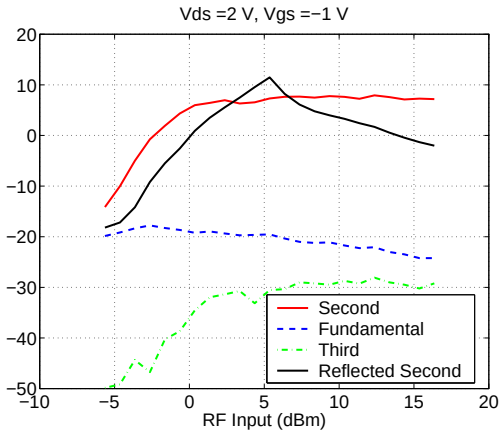


Fig. 4. Measured output and reflected power of the 20.8 GHz doubler as a function of input RF power.

shown in Fig. 4 together with the output power. Also shown are the efficiencies corresponding to the different power levels. This data shows that there is a considerable reflected second harmonic content. Around the point of maximal efficiency at 6.3 dBm input power, the reflected second harmonic power is 8.2 dBm, which is larger than the output power.

VI. Discussion

We have shown that class-E multiplier design can be extended to K-band with commercial transistors to obtain high DC-RF (42.7%) and overall (31.6%) efficiency with 0.83 dB conversion gain. 5.23 dB conversion gain and 5.5 dBm output power can be obtained at a moderate 23.5% overall efficiency. Measurements indicate that when no input harmonic tuning is applied, approximately half the generated harmonic power is reflected towards the input. The conversion gain and efficiency of the multiplier could be improved significantly if proper harmonic filtering is used.

VII. Acknowledgements

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