Micro-Bias-Tees Using Micromachined Flip-Chip Inductors

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Abstract— **In order to reduce the circuit area required by bias-tees in active circuits, an approach using a micromachined suspended inductor is presented in this paper. The inductor is fabricated using a commercial silicon micromachining process and then integrated with a microwave circuit using flip-chip assembly. Suspending the inductor above the substrate greatly reduces the parasitic capacitances associated with the substrate. The inductor has a measured self-resonant frequency of 18 GHz. A tethered approach allows "pre-releasing" of the structure, which makes integration possible on *any* substrate. 4-mm^2 bias-tees on both alumina and TMM6 substrates are presented in this work with comparable performance to commercially available bias-tees, but with a significant reduction in circuit area.**

I. Introduction

Bias-tees are an essential component in active microwave circuits, providing both DC power to transistors and control signals to switches and MEMS devices. In RF applications, bias-tees must provide high isolation and low return loss in order to supply DC with little effect on high-frequency performance. The impedance of the DC line must be high to prevent loading, usually requiring an inductor as an RF choke.

Currently, RF front-end circuitry is heavily dependent on large, off-chip, discrete passive components. Conventional integrated planar inductors are severely limited by parasitic effects due to the substrate. These parasitics may be reduced through bulk substrate removal below the inductor [1]-[2], surface micromachining of a suspended electroplated inductor [3]-[4], or self-assembly of inductors oriented at larges angles with respect to the substrate surface [5]-[7].

An alternative approach presented here is to fabricate a micromachined inductor on a SiO_2 sacrificial layer and silicon host wafer using a standard commercially available surface micromachining process. A flip-chip process transfers the inductor to gold bumps on *any* receiving microwave substrate. The resulting inductor structure is suspended on gold bumps 60 μm above the substrate, greatly reducing parasitic losses.

MEMS releasing processes require strong acids, usually containing hydrofluoric acid (HF), which damage most microwave substrates and integrated devices. To allow integration on any substrate, possibly already containing RF circuitry and devices, these inductors are "pre-released" before integration with the microwave substrate. Pre-releasing is accomplished using "tethers" to anchor the structure to the silicon host wafer, allowing etching of the sacrificial layer before integration. In the flip-chip process, the tethers break at designed points during the bonding, resulting in a micromachined structure bonded to the receiving substrate, free of the low resistivity silicon host wafer.

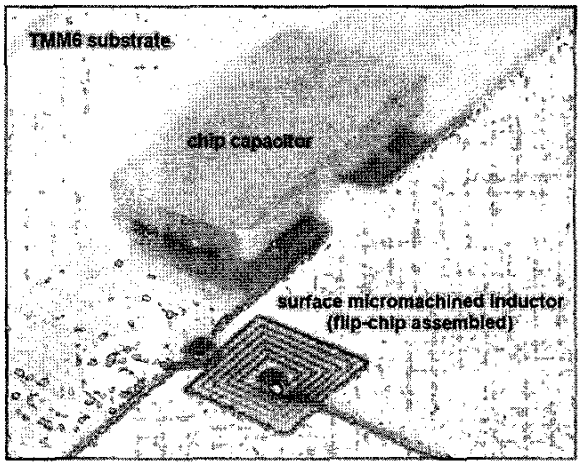

Fig. 1. A photograph of a broadband micro-bias-tee. A 18 nH micromachined inductor, flip-chip integrated on TMM6, and suspended 60 μm above the substrate provides the RF choke. A commerical 8.2 pF chip capacitor is the DC block. The RF input and output microstrip lines have a characteristic impedance of 50 Ω, and the DC input line has a characteristic impedance of 110 Ω. This bias-tee requires only 4 mm^2 of circuit area.

The bias-tees developed in this work use silicon-gold micromachined inductors integrated on both alumina (Al_2O_3, $\epsilon_r = 9.8$, $t = 25$ mil) and Rogers TMM6 ($\epsilon_r = 6$, $t = 25$ mil, shown in Fig. 1). The circuit area required for these bias-tees is only 4 mm^2, significantly smaller than commercial bias-tees. Micro-bias-tees enable dense integration of high microwave frequency circuits.

II. Inductor Design and Fabrication

The inductor is fabricated using surface micromachining in the MEMSCAP Multi-User MEMS Process (MUMPs). Poly-silicon and trapped oxide layers are used for structural support, with a gold metalization layer as

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a low-loss conductive path. Unfortunately, limitations in the metal thickness available in process used (0.5 μm) prohibit the design of a gold layer greater than the skin depth (0.79 μm at 10 GHz). This limitation can result in reduction of the Q-factor. Electroplating can reduce series resistance due to the thin conductive poly-silicon.

The inductor coil is 20 μm wide, with outer dimensions of 650x650 μm^2, and supported by two 100x100 μm^2 bond pads.

Several terms are essential to understanding the assembly of this inductor:

- **host substrate:** low-resistivity silicon used for device fabrication, not suitable for microwave circuits (hence, it is necessary to remove it)
- **receiving substrate:** *any* substrate with good RF performance characteristics, however typically not compatible with micromachining and MEMS fabrication processes
- **gold bumps:** used to connect the flip-chip device to the receiving substrate
- **flip-chip:** a method of bonding a "flipped" device to a receiving substrate
- **pre-releasing:** etching of the sacrificial layer before integration with the circuit, requiring tethers to complete the transfer from host to receiving substrate
- **tether:** integrated assembly structure fabricated simultaneously with the device on the host substrate and designed to break during the flip-chip assembly, transferring a pre-released device from the host substrate to the receiving substrate without using *any* etchants

To facilitate transfer to a wide variety of substrates, including those with pre-existing RF circuitry and semiconductor devices, a tethering technique allows pre-releasing of an anchored inductor. The tether is a poly-silicon structure connected initially to the device and anchoring it to the host substrate. It is used solely for device assembly. These tethers are designed to break at specific points during the flip-chip process [8]. Previous related work in flip-chip transfer and tethering specifically designed for mounting on quartz substrates is presented in [9]-[12].

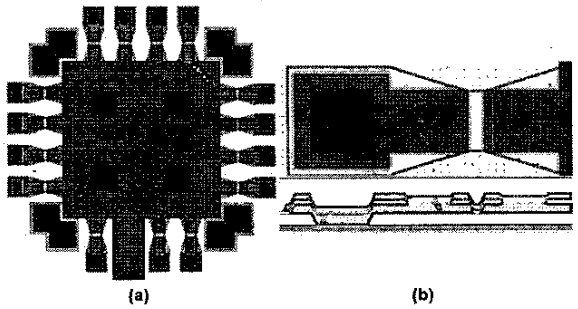


Fig. 2. Tethers surrounding a bond-pad (a) and an enlarged top and cross sectional view of a single tether (b). The notch is located at a predetermined breaking point.

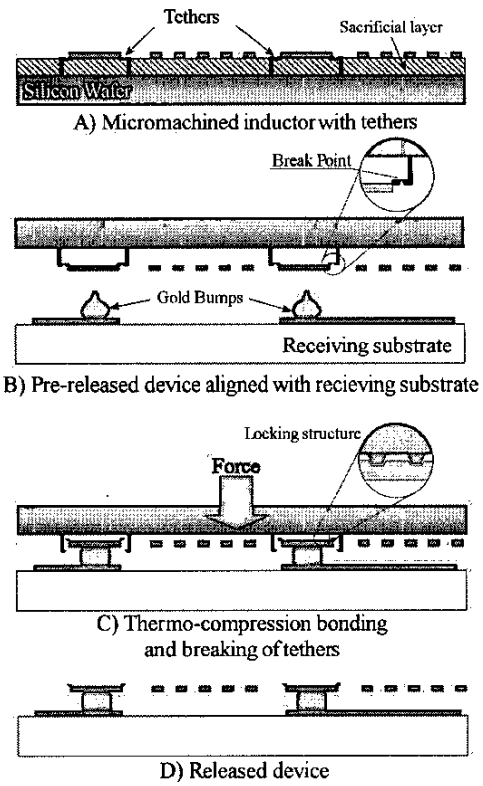
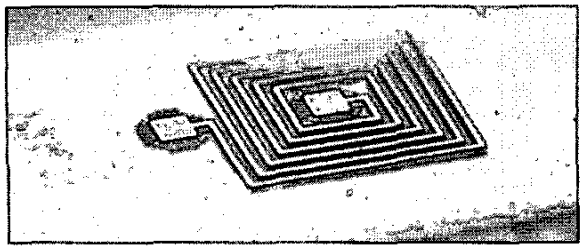
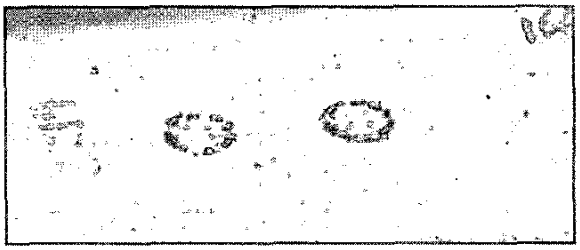


Fig. 3. A cross-sectional illustration of the pre-release and flip-chip transfer process of the tethered inductor. The sacrificial oxide layer of the host wafer with micromachined inductor features (a) is etched, leaving the inductor structure anchored to the host substrate by the tethers. The inductor-host substrate combination is then flipped and aligned (b) with the gold bumps on the receiving substrate. Thermo-compression bonding (c) joins the inductor bond-pads to the gold bumps and simultaneously breaks the tethers at designed points. The inset in (c) shows an interlocking structure to hold the inductor in place during the bonding process. After flip-chip transfer, the resulting structure is a released device (d).

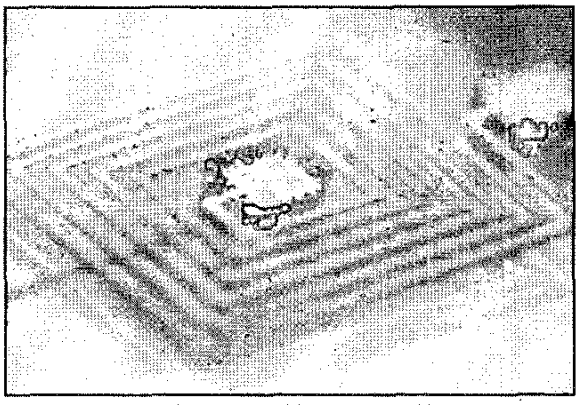
The tethers are located around the bond-pads, which are the locations of maximum pressure during the thermo-compression bonding process. Each tether is designed with a notch, which is a stress concentration point and the breaking point during bonding. Fig. 2 illustrates top and cross sectional views of the tethers surrounding the bond-pad of the inductor. The pre-release and tethered flip-chip assembly process is illustrated and described in Fig. 3, and shown photographically in Fig. 4.



(a) A pre-released inductor anchored by tethers to the host silicon substrate.



(b) Broken tethers remaining on the host substrate after flip-chip assembly.



(c) Final integrated inductor assembly.

Fig. 4. The micromachined inductor on the host silicon wafer after pre-release (a). The gold layer is visible on the surface of the inductor. After flip-chip bonding, the tethers break away from the inductor structure and remain attached to the host wafer (b). The final structure is a suspended inductor (c). The top layer visible on the inductor in (c) is polysilicon. The gold layer is now underneath the structure.

III. Bias-Tee Design Characterization

A higher microwave frequencies, lack of quality inductors imposes narrowband, relatively large transmission line stubs in bias-line design. A high resonant frequency miniature inductor with an inductance greater than 5 nH would provide a 300 Ω impedance at RF frequencies larger than 10 GHz. As a demonstration of the 18 nH inductor and the versatility of the tether transfer, bias-tees on alumina and TMM6 standard microwave substrates are developed. A bias-tee consists of a DC blocking capacitor (a short for RF) and an inductor (a high impedance for RF). In the design presented here, the inductor is used in a tee configuration with an 8.2 pF ATC chip capacitor.

Using a coplanar waveguide (CPW) probe station and an HP8510C network analyzer with TRL calibration, the self-resonant frequency of the inductor was measured to be 18 GHz. The bias-tees were fabricated including CPW to microstrip transistions from JMicroTechnology in order to use the same calibration standards. The insertion loss (S_{21}) and the return loss (S_{11}) were measured. The return loss was less than 7 dB for frequencies below 25 GHz on both substrates.

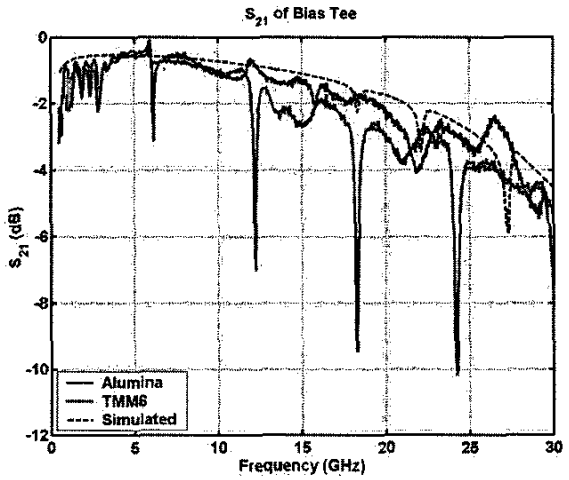


Fig. 5. Insertion loss (S_{21}) of the bias-tee for both alumina and TMM6 substrates, compared with simulated values.

The measured insertion loss is shown in Fig. 5. It is heavily dependent on the parasitic inductance associated with the DC blocking capacitor, which is 0.4 nH for the commercial device used here. Reducing this parasitic inductance to 0.2 nH gains 1 dB of improvement at 10 GHz and 3 dB of improvement at 30 GHz, according to simulations.

One undesired feature of these bias-tees are the resonances at 12, 17, and 24 GHz in the TMM6 circuit. These resonances also occur in the simulation, though at different frequencies. Although the inductor has greatly reduced parasitic capacitances by suspending it above the substrate, it is not an ideal inductor. At these frequencies, the impedance of the inductor drops significantly, reducing the overall impedance of the DC bias line. Improvements in the inductor's equivalent circuit model will better predict these points of low impedance and aid in reducing their effects.

The DC current handling ability of these micro-

machined inductors was also measured. First signs of warpage begin at 50 mA. This warpage is due to current heating effects in the inductor, causing thermal stress between the gold and poly-silicon layers. Increasing the thickness of the metal layer by electroplating or an alternative micromachining process would reduce the series resistance of the inductor and allow larger currents.

One goal of this work was to make the bias-tee electrically comparable to a commercial bias tee. For comparison, characteristics of this bias-tee are listed with the characteristics of a Picosecond Pulse Labs 5545 Bias Tee [13] in Table I. The values listed here are for the alumina bias-tee, which does not exhibit strong resonances. We feel that the resonances can be removed in future circuit generations. It should be noted that the Picosecond bias-tee values include losses in the SMA connectors on the order of 0.1-0.2 dB.

TABLE I
COMPARISON WITH A COMMERCIAL BIAS-TEE

	Micro-Bias-Tee	**Picosecond 5545**
Bandwidth (-3 dB)	20 GHz	20 GHz
Capacitance	8.2 pF	0.03 μF
Inductance	18 nH	340 μH
Insertion Loss		0.7 dB typical
	<1 dB, f<10 GHz	<1 dB, f<5 GHz
	<1.5 dB, f<15 GHz	<1.5 dB, f<12 GHz
Return Loss		23 dB, f=100 MHz
	>15 dB, f<10 GHz	>20 dB, f<6 GHz
	>10 dB, f<24 GHz	>12 dB, f<14 GHz
DC Current	50 mA	500 mA
Connectors	Integrated	SMA
Dimensions	2.25x1.8x0.2 mm^3	2.54x2.54x1.6 cm^3
Area	4 mm^2	6.45 cm^2

IV. CONCLUSION AND DISCUSSION

The micro-bias-tee presented in this work has comparable electrical performance to commerical bias-tees, with a significant reduction in circuit area, but lower current handling capability. The area is reduced by a factor of 100, while the current is reduced by a factor of 10. The small size of the inductors allows topologies with multiple inductors in series and parallel combinations to double the current delivered to the circuit without changing the inductance.

The measured inductance is 18 nH, and the measured self-resonant frequency of these micromachined inductors is 18 GHz. These inductors are capable of handling 50 mA before being damaged by current heating. The metal layer available in the MUMPs process is thinner than the skin depth, which increases the series resistance of the inductor and lowers the Q (although the inductor Q-factor is not critical for this particular application). Based on measured series resistance the Q-factor is estimated to be around 40. Electroplating techniques will provide a higher Q and larger current handling capabilities.

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