60% Efficient 10-GHz Power Amplifier With Dynamic Drain Bias Control

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***Abstract*—This paper describes the design, implementation, and characterization of a high-efficiency 10-GHz amplifier with dynamic drain bias control that maintains high efficiency over a range of output power levels. The power amplifier (PA) operates in class-E switched mode with 67% drain efficiency at an output power of 20.3 dBm, 0.7 dB less than the specified maximum power for the device. A coupler and detector at the output of the PA provide a feedback signal to the drain-bias controller based on a 96% efficient Buck dc–dc converter. When compared with a PA with constant drain bias (4 V), the average efficiency of the PA with dynamic biasing is improved by a factor of 1.4. Over an output power between 15–20 dBm, the drain bias varies from 2 to 4 V, and the efficiency improves from 22% to 65% at the lower power level. The efficiency includes the losses in the dc–dc converter.**

***Index Terms*—dc–dc converter, dynamic biasing, high efficiency, power amplifiers (PAs).**

I. Introduction

HIGH-EFFICIENCY power amplifiers (PAs) are designed to operate in the saturated regime. As a consequence, when a range of output power levels is required, such as in the case of mobile phone communications, the efficiency suffers at the lower power levels. The idea of dynamic control of the bias supply is brought up to increase the efficiency for low output power levels by optimally varying the bias supply [1]–[7]. Hanington *et al.* [4] designed a dynamic control circuit using a boost dc–dc converter, and demonstrated an increase in average efficiency by a factor 1.64 (from 3.89% to 6.38%) for a 1-MHz bandwidth code-division multiple-access (CDMA) signal input to a 950-MHz HBT class-A PA. The same authors applied a digital signal processor (DSP) controlled dc–dc converter and a predistortion technique to a 950-MHz CDMA signal amplifier and showed improvement in efficiency (by a factor of 1.4), as well as linearity (8-dB improvement in adjacent channel power ratio) [5]. Staudinger *et al.* [6] and Raab *et al.* [7] used a class-S modulator to supply the dynamic changing drain bias at low microwave frequencies (835 MHz and L-band). In [6], the average efficiency for CDMA signals was increased by a factor of five over the constant bias case.

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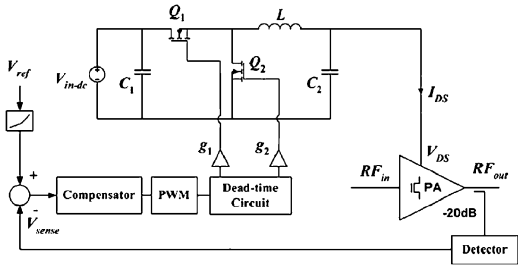

Fig. 1. Switched-mode PA with closed-loop power control using dynamic drain bias.

The goal of this paper is to demonstrate very high peak efficiency (over 60%), as well as improved average efficiency over a range of output power levels of an X-band PA. The 10-GHz design frequency is ten times higher than the carrier frequencies in [1]–[7], making the high-efficiency switch-mode design more difficult. The block diagram of the dynamically biased class-E PA is shown in Fig. 1. A coupler/detector circuit at the output of the PA provides a reference feedback signal to the controller of a high-efficiency Buck dc–dc converter. The PA, detector, controller circuit, and dc–dc converter are characterized separately, and then in a complete feedback circuit.

II. Class-E Amplifier Design

In a class-E switched mode PA, the transistor is biased to operate as a switch and ideally offers 100% efficiency [8], [9]. The class-E mode was extended to microwave frequencies in a transmission-line circuit in 1995 [10]. The optimal class-E mode of operation requires the load to be open circuited for all harmonics with a fundamental-frequency impedance of

$$Z_E = \frac{0.28}{\omega_S C_{\rm OUT}} e^{j49^\circ} \tag{1}$$

where $C_{\rm OUT}$ is the output capacitance of the transistor at the fundamental angular frequency ω_S. The finite resistance during the ON state of the transistor and finite switching speed makes the ideal 100% efficiency impossible to achieve, but nevertheless, very high efficiencies around 70% are attainable at X-band [11], [12].

The 10-GHz class-E PA used in this study adopts the same design as in [12], where 16 such PAs are combined in a spatial power combiner with 80% combining efficiency. The PA uses a commercial GaAs MESFET from Alpha Industries, Woburn, MA, that can operate in suboptimal class-E mode at 10 GHz

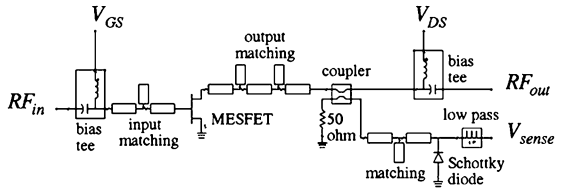

Fig. 2. Microwave portion of the dynamically controlled PA circuit, includes the PA with input and output matching circuits, biasing circuits, and output power detector (coupler, Schottky diode, and low-pass filter).

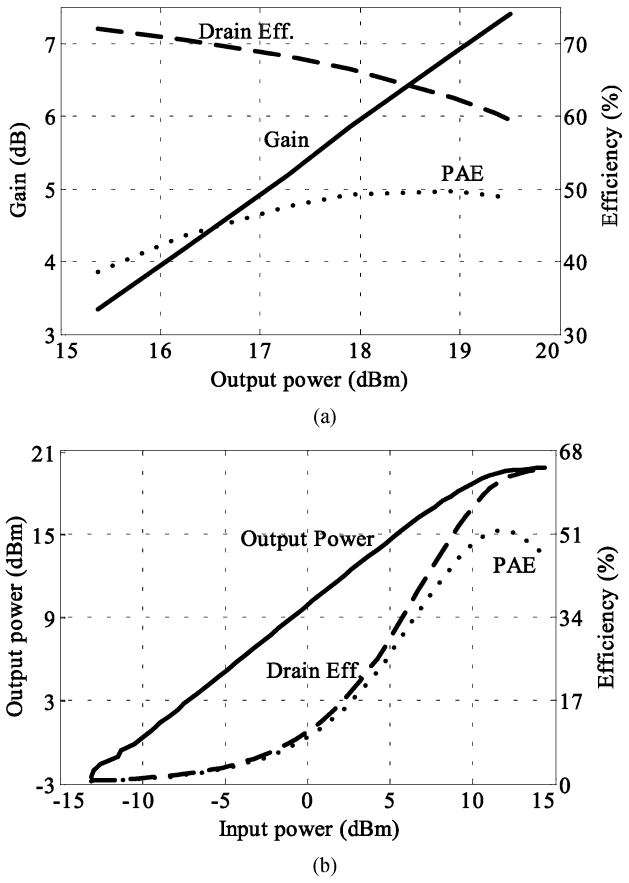

Fig. 3. Measured characteristics of the class-E PA element. (a) Gain and efficiency as a function of output power. (b) Output power and efficiency as a function of input power.

with a drain efficiency around 70%. The efficiency is above 60% over a 14% bandwidth with output power flatness of 0.5 dB [12].

The microwave portion of the dynamically biased PA circuit is shown in Fig. 2. The PA output network consists of two stubs, one that provides the open-circuit termination for the second harmonic and the other the desired load at the fundamental frequency. The input matching network maximizes the compressed amplifier gain. The substrate used in the PA implementation is Rogers TMM6 with $\varepsilon_r = 6$ and a thickness of 0.635 mm. The chip device is mounted on a ground pedestal to minimize bond-wire inductances. Fig. 3 shows the measured power, efficiency, and gain of the PA in terms of input and output power. The results in Fig. 3(a) are measured for a fixed input power of 12 dBm, gate bias of -1.4 V and varying drain bias. The output power and efficiency in Fig. 3(b) are measured with a gate bias of -1.4 V, a drain bias of 4.0 V and varying input power.

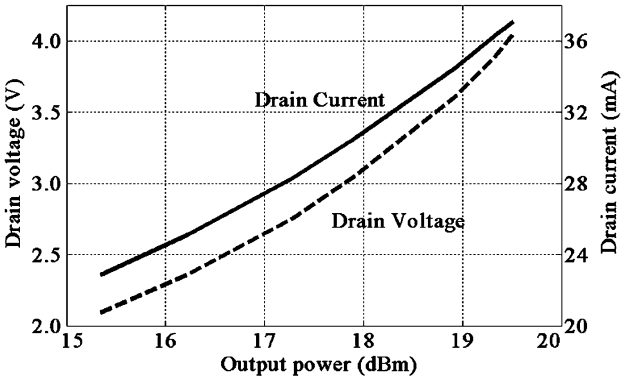

Fig. 4. Measured drain voltage and current of the PA versus output power for constant input power.

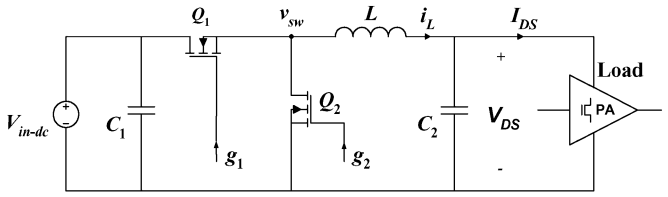

Fig. 5. Power stage of the synchronous buck converter. The range of input dc voltage is 5–7 V, $C_1 = C_2 = 10\ \mu$F, $L = 10\ \mu$H, and the load is the class-E microwave PA drain terminal. The MOSFETs used in this implementation are IRF7331.

The PA drain bias properties are also characterized in order to define the operating range for the dc–dc converter. For the case of power control presented here, the measured dependence of $I_{\rm DS}$ and $V_{\rm DS}$ over a range of output powers is recorded in Fig. 4, and this information provides the reference for the design of the power control feedback loop shown in Fig. 1.

To sense the output power, a 20-dB coupled-line coupler and a single-diode detector follow the output PA matching circuit. The insertion loss of the coupler is less than 0.5 dB, with connectors contributing approximately 0.2 dB in addition. An Agilent HSCH-5332 Schottky diode is used for the detector. Input matching is provided by a single stub and, at the output, the 10-GHz signal is filtered to obtain the signal $V_{\rm sense}$. In the feedback loop, this signal is compared with a reference $V_{\rm ref}$, which serves as the power command signal. The loop is closed through the dc–dc converter that adjusts the drain bias to the PA such that the measured output power signal matches the command power signal.

III. Dynamic Drain-Bias Control Circuit

The drain-bias voltage of the PA is provided by a synchronous dc–dc buck converter shown in Fig. 5. This converter is the most preferred configuration in low-voltage step-down applications because the relatively low voltage drop across the synchronous rectifier reduces conduction losses [13]. The filter inductor ($L = 10\ \mu$H) is selected so that the inductor current ripple results in zero-voltage switching of the MOSFETs Q_1 and Q_2 [13]. As a result, switching losses in the converter are reduced. Following design guidelines for optimization of the total switching loss, which results in a tradeoff between conduction and switching losses [14], the IRF7331 MOSFETs Q_1 and Q_2 and the switching frequency $f_s = 200$ kHz are selected to maximize

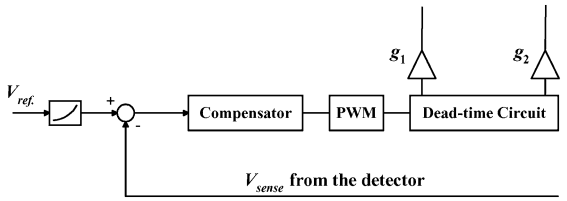

Fig. 6. Self-assessment signal $V_{\rm sense}$ from the detector at the output of the PA is compared with a pre-measured power reference signal $V_{\rm ref}$ obtained by characterizing the PA. The PWM generates the gate-drive control signals g_1 and g_2 for the MOSFETs Q_1 and Q_2 from Fig. 1.

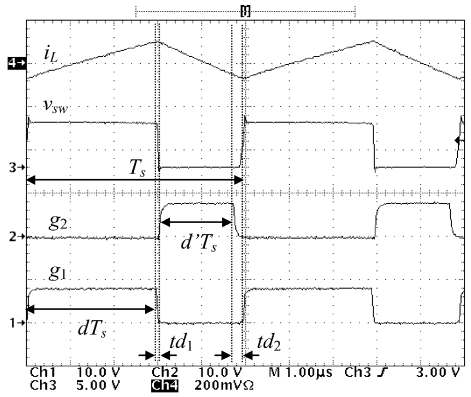

Fig. 7. Measured waveforms in the synchronous buck converter. Trace 1: gate drive signal g_1. Trace 2: gate drive signal g_2. Trace 3: Q_2 drain voltage $v_{\rm sw}$. Trace 4: inductor L current i_L (200 mA/div). The switching frequency is $f_s = 200$ kHz with an output voltage $V_{\rm DS} = 3$ V and load current $I_{\rm DS} = 30$ mA.

the efficiency of the converter over the operating range shown in Fig. 4. The low effective series resistance output filter capacitor ($C_2 = 10$ μF) results in negligibly small switching ripple in the drain bias voltage $V_{\rm DS}$.

The control circuitry of the dc–dc is shown in Fig. 6. The self-assessment signal $V_{\rm sense}$ from the detector at the output of the PA is compared with a pre-measured power reference signal $V_{\rm ref}$ obtained by characterizing the PA. The output of the comparator is the error signal, which is integrated by the compensator for precise steady-state output power regulation.

The output of the compensator is the input to a pulsewidth modulator (PWM), which generates the gate-drive control signals g_1 and g_2 for the MOSFETs Q_1 and Q_2. Fig. 7 shows experimental waveforms in the synchronous buck converter: the inductor current i_L, switching waveform $v_{\rm sw}$, and gate-drive signals g_1 and g_2.

During the dT_s portion of the switching period T_s, the MOSFET Q_1 is turned on and the inductor current ramps up. When the MOSFET Q_1 is turned off, the inductor current discharges the parasitic capacitance at the $v_{\rm sw}$ node. After a short delay td_1, the switching voltage $v_{\rm sw}$ drops to zero, and the synchronous rectifier Q_2 is turned on at zero voltage. During the $d'T_s$ portion of the switching period, the MOSFET Q_2 is on and the inductor current ramps down. At the end of the $d'T_s$ interval, the inductor current has reversed polarity. As a result, when Q_2 is turned off, the inductor current charges the parasitic capacitance at the $v_{\rm sw}$ node, which allows zero-voltage turn-on of the MOSFET Q_2 after a short delay td_2. The necessary delays td_1 and td_2 are created by the dead-time circuit block shown in Fig. 6. The zero-voltage-switching quasi-square-wave

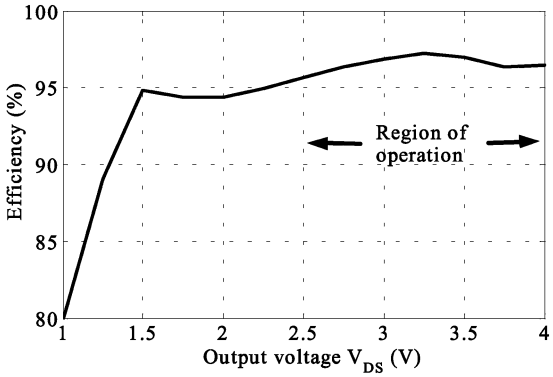

Fig. 8. Measured efficiency of the dc–dc converter as a function of the output voltage $V_{\rm DS}$ for the PA as the load.

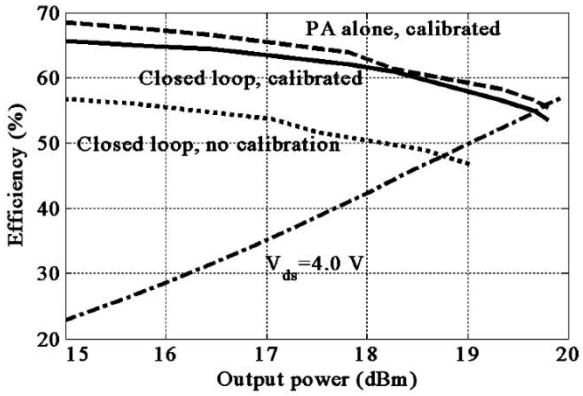

Fig. 9. Measured efficiency for the PA with constant drain bias (dashed–dotted line), the PA with manual drain bias control (dashed line), the entire closed-loop system when the connector loss and coupler loss is calibrated out (solid line), and the uncalibrated closed-loop system (dotted line).

operation described above results in reduced switching loss and improved efficiency of the converter [15].

The measured efficiency of the dc–dc converter with the PA as the load is shown in Fig. 8 as a function of the output voltage $V_{\rm DS}$, which is the drain-bias voltage for the PA. For load currents greater than 15 mA and output voltages greater than 1.5 V, the efficiency is above 95%. In the operation region of the PA, which is indicated in Fig. 4, the dc–dc converter efficiency is greater than 96%.

IV. Closed-Loop Dynamic Bias Control of PA

The entire dynamically biased PA, as shown in Fig. 1, is implemented in a hybrid circuit and characterized. The sensed voltage $V_{\rm sense}$ at the output of the detector is compared to the power reference voltage $V_{\rm ref}$. Changes in the output power induce changes in the duty cycle of the converter and, hence, the drain bias and the output power is regulated to the specified reference value. The efficiency of the PA with the closed-loop power control and with constant input power of 12 dBm is measured and is shown in Fig. 8 over the output power range of 15–20 dBm. The gate-bias voltage is kept at -1 V.

Several curves are compared in Fig. 9. The curve with the lowest overall efficiency is measured for constant drain bias, while the output power is varied. The highest efficiency curve,

with an average drain efficiency of 62.3%, is measured for the PA alone where the drain bias is varied manually. The solid line with an average efficiency of 60.4% is obtained with the entire closed-loop circuit from Fig. 1 and the loss due to the connectors and coupler calibrated out. The dotted curve shows the slightly lower measured total efficiency that includes the connector loss, which can easily be eliminated by fabricating the PA and coupler/detector circuit on the same substrate.

The average efficiency is calculated from measured data as an unweighted average, and a summary is as follows:

$$\begin{aligned}\eta_{\mathrm{PA}} &= 62.3\% \\ \eta_{\mathrm{loop}} &= 60.4\% \\ \eta_{\mathrm{loop,connectors}} &= 50.7\% \\ \eta_{\mathrm{constant}\ V_{\mathrm{ds}}} &= 41.5\%\end{aligned}$$

where η_{PA} is the drain efficiency of the class-E PA at optimal bias and constant input power, η_{loop} is the efficiency of the entire closed loop for the same conditions, $\eta_{\mathrm{loop,connectors}}$ is the measured efficiency that includes the coupler and connector losses, and $\eta_{\mathrm{constant}V_{\mathrm{ds}}}$ is the efficiency of the PA for constant drain bias and varying input power. The final conclusion of the work presented in Fig. 9 is that the average efficiency is increased by a factor of 1.46 when efficient dynamic biasing is used in the feedback loop of an efficient PA, assuming a uniform power probability distribution. The effect would be more dramatic for a low-efficiency PA and for signals that have more occurrences of lower power levels. For any other probability density function of power distribution, the corresponding improvement can be calculated from the curves in Fig. 9.

V. Conclusion and Discussion

In summary, this paper has presented a 10-GHz class-E PA with a dynamic drain bias control that allows efficient operation over a range of output power levels. The efficiency, averaged over the output power range, is increased from 41.5% to 60%, including the losses in the adaptive dc–dc converter. The PA includes a coupler/detector self-assessment circuit at the output port, and is pre-characterized to provide a reference voltage function for bias optimization.

It is relevant to compare the heat dissipation for the PA with and without dynamic bias control. For a uniform probability distribution function of the output power in the given range, the constant-drain bias PA dissipates 88 mW on average, while the dynamically biased PA dissipates 45 mW, or around a factor of two less.

This paper has demonstrated one possible optimization process using dynamic biasing, namely, maintaining high efficiency over a range of output powers. Clearly, for applications that require very high linearity (e.g., CDMA), this highly compressed PA mode is not suitable. The method, however, is quite general, and other PA improvements under current development are gate-bias control for temperature stabilization, bias control for increasing average efficiency for input signals with varying envelopes, and bias control for linearity.

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