A Low-Power, Low Phase Noise Local Oscillator for Chip-Scale Atomic Clocks

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***Abstract* — This paper presents a voltage controlled oscillator (VCO) for application in chip-scale atomic frequency references. At 3.4GHz (half of the Rubidium atom ground-state hyperfine transition frequency), the VCO demonstrates low phase noise (-33dBc@100Hz and -92dBc@10kHz) at 4.5mW power consumption with a circuit footprint <0.5cm^2. The temperature stability is 0ppm/°C at room temperature, and does not exceed -40ppm/°C over the range of -5°C to +65°C. Locking to the Coherent Population Trapping (CPT) resonance of a NIST Rb clock is enabled by a weakly-coupled varactor diode which provides ~3MHz of tuning range. The oscillator is implemented using low-cost off-the-shelf surface-mount components, including a micro-coaxial resonator. To the authors' knowledge, this VCO has the lowest simultaneous size, phase noise, DC power consumption and thermal drift published in the literature.**

***Index Terms* — Atomic clocks, microwave bipolar transistor oscillators, coaxial resonators, phase noise, varactor tuning, vertical cavity surface emitting lasers, VCSEL, voltage controlled oscillators.**

I. Introduction

Recently there has been increased interest in ultra-miniature atomic clocks as time references for both military and commercial applications such as anti-jam GPS, synchronization in communication networks, and encryption [1,2]. The ultimate goal is a chip-scale atomic clock (CSAC) which includes a glass cell containing atoms, a vertical-cavity surface-emitting laser (VCSEL) at the optical resonant wavelength of the atoms, a photodetector, associated optics, a microwave VCO which locks to the atomic CPT resonance, thermal management and locking circuitry, all in a 1-cm^3 package [3]. The power consumption for the entire clock is desired to be a maximum of 30mW, most of which is dedicated to thermal management. With these requirements, a fractional frequency instability below 10^{-11} is desired at one-hour integration times and longer [3].

Briefly stated, an atomic clock is a frequency reference that gives an extremely pure periodic signal at the hyperfine transition frequency of the particular atom species. The most commonly used atoms are those of Rubidium and Cesium, for which the ground-state hyperfine transition frequencies are 6.834683GHz and 9.192632GHz, respectively. In order to maintain the resonance, a very stable microwave VCO at either the atomic resonant frequency or half of this frequency is usually required [3]. The VCO is locked to the CPT resonance, combining the short-term stability of the VCO with the long-term stability of the atoms. In this paper, a 3.4-GHz VCO for a chip-scale Rubidium clock is discussed. The output of the VCO is designed to modulate a VCSEL diode so that the sidebands on the beam passing through a 1mm^3 Rb gas cell will be separated by exactly the atomic ground-state hyperfine transition frequency.

The goals for the VCO of a chip-scale atomic clock can be summarized as follows:

- Expected phase noise better than –25dBc/Hz@100Hz offset (calculated from the total package fractional frequency instability requirement of 10^{-11} for a 1 hour integration time);
- Output power at –6dBm when assuming the VCSEL presents a 50-Ω load (as this is not the case, simply matching for the load will allow even lower power output);
- Small footprint of <1cm^2, fabricated on one side of a thin substrate;
- Low DC power consumption of at most 10mW;
- Low thermal frequency drift on the order of ±10ppm/°C;
- A frequency tuning range that is as small as possible but large enough to compensate for thermal drift over large temperature ranges and for manufacturing tolerances;
- Low-cost manufacturability for high yield.

The VCO presented in this paper is designed with surface-mount standard components and uses a very small coaxial resonator as the high-Q element. The design and characterization of the VCO are presented in the remainder of the paper.

II. Oscillator Design and Fabrication

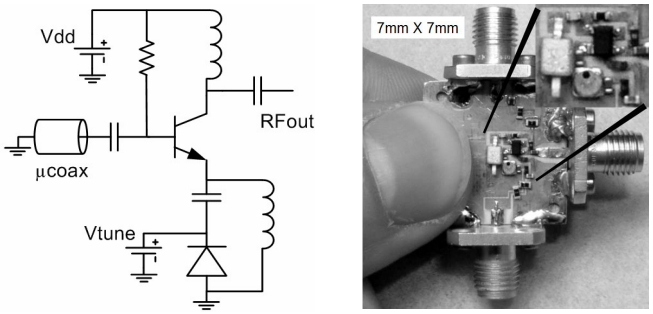

Fig.1. Simplified circuit diagram (a) and photograph of VCO (b). The circuit is coplanar and fabricated on a Rogers 4350 substrate. The high-Q element is a surface-mount, quarter-wave, shorted micro-coaxial resonator manufactured by PicoFarad, and the capacitors, inductors and varactor are standard surface-mount components.

The oscillator (Fig. 1) is a series resonant feedback topology, with the resonator capacitively coupled off the base of a Si BJT (Infinion BFP405). A weakly-coupled varactor diode provides the 3-MHz tuneability required to compensate for thermal drift and some manufacturing tolerances. It was designed using Agilent's Advanced Design System (ADS) harmonic-balance software and a simplified circuit diagram is given in Fig. 1a. ADS harmonic-balance permits analysis for specific output power levels and phase noise, which were critical to this design. However, simulated phase noise (Fig. 2) was only valid at large offset frequencies since the transistor noise model did not account for the flicker noise corner. Models for the transistor and varactor were provided by the manufacturers and we developed a simple resonator model based on size, material properties, and measured data of the loaded and unloaded Q factor. The micro-coaxial resonator has a measured unloaded Q factor of approximately 250 and in this design it is critically coupled to the circuit with a resulting loaded Q estimated to be 125.

All of the components are surface-mountable and well-suited for standard reflow soldering and most are size 0402 packages, chosen to meet the small size requirement. The transistor (Infineon BFP405) is chosen because of its low noise and high gain at microwave frequencies, enabling a low-power, low phase noise design. A λ/4 ceramic-filled coaxial resonator is chosen because of its high Q, small size (2mm by 2mm by 3.9mm) and good thermal stability (+7ppm/°C). Such resonators exhibit an improvement in size, temperature stability, and vibration sensitivity over most quartz resonators and more than three times better stability over wide temperature variations than recently produced high-Q film bulk acoustic resonators (FBARs) [4,5]. As price is also a consideration for CSACs, the surface-mount coaxial resonators (several dollars per resonator, depending on frequency, size, and quantity) [6] are a good choice but remain the largest component expense in the design.

The VCO is fabricated on the top layer of a standard substrate (Rogers 4350) which allows for the necessary CSAC locking and thermal control circuitry to be integrated on the bottom layer, with vias carrying control voltages to the VCO and to MEMS heaters on the Rubidium gas cell and VCSEL.

III. Experimental Results

TABLE I
COMPARISON OF DC BIAS POWER TO RF OUTPUT POWER

Bias Voltage	Bias Power	RF Output Power
1.90V	7.6mW	2dBm
1.50V	4.5mW	-2dBm
1.30V	2.8mW	-5dBm
1.20V	2.1mW	-6dBm
1.00V	0.7mW	-16dBm

A. DC Power Consumption and RF Power Delivered

The power necessary to optimally modulate the VCSEL in the Rubidium-based CSAC at the National Institute of Standards and Technology (NIST) is approximately -6dBm, when delivered into a 50-Ω load [7]. It is likely that the required power for an impedance-matched, predominantly reactive-impedance VCSEL will be lower. Since the power requirement is panning out to be the most stringent for this project, and since modulating the VCSEL with either too little or too much power does not generally work, our goal is to deliver exactly the required power as efficiently as possible while maintaining very low phase noise.

Table 1 shows the measured DC input power corresponding to measured RF output power levels. Our desired output power of -6dBm requires approximately 2.1mW of DC power at 1.2V. The low efficiency of around 10% is a trade-off to achieve lower phase noise.

B. Phase Noise

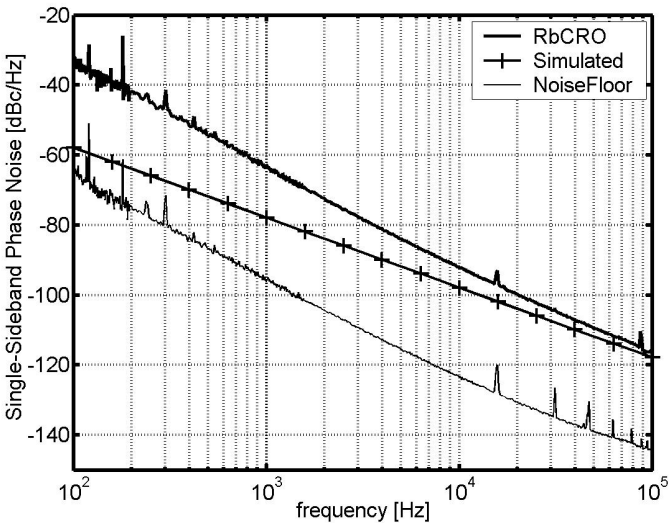

Fig. 2. Measured phase noise of 3.4GHz VCO compared to ADS harmonic balance simulation. The phase-noise floor is shown to verify the feasibility of the measurement system.

The phase noise is measured directly using the discriminator method [8] with a 125ns low-loss coaxial delay line. The measurement is verified by evaluating a commercial DRO and comparing to the DRO characteristics obtained using an Agilent E5500 phase noise measurement system. This measurement technique enables phase noise measurements down to -115dBc/Hz at 10kHz offset at fundamental frequencies of up to 10GHz. The noise floor in Fig. 2 is shown to be sufficiently low to permit our measurements.

For this measurement, the output signal from the oscillator is amplified to produce approximately 17dBm of output power. Half of this power is sent to the LO port of a low-noise mixer and the other half through a delay line and phase shifter. This signal is mixed in quadrature at the RF port of the mixer

and the IF output is amplified and measured by a Stanford Research Systems SR760 FFT spectrum analyzer.

The oscillator is measured at a bias voltage of 1.5V and shows little degradation as the bias is decreased to 1.1V. As shown in Fig. 2, the phase noise measured at a 10kHz offset is less than -92dBc/Hz. The close-in phase noise is -33dBc/Hz at a 100Hz offset. This is an improvement over the current phase noise requirement of -25dBc/Hz at 100Hz offset, which is calculated from a fractional frequency instability requirement for the completed CSAC of 10^{-11} at a one-hour integration time, assuming the phase noise goes as $1/f^3$, a locking time of 10ms, and a 1-pole response in the feedback locking circuitry from the photodetector (Fig. 4).

These results are an improvement over other small-sized, low phase noise oscillators currently available in the literature for CSAC: State-of-the-art free-running MMIC oscillators typically have low power but a modest phase noise of approximately -80dBc at 10kHz offset [11]. A notable exception [12] combines an off-chip FBAR resonator with integrated CMOS. Unfortunately, for CSAC applications, the oscillator was not tunable and the low power was quoted for the oscillator core only. Considering a recent design [5], FBAR-resonator oscillators may prove suitable for this application if DC power consumption is reduced and thermal frequency drift is compensated.

C. Thermal Drift

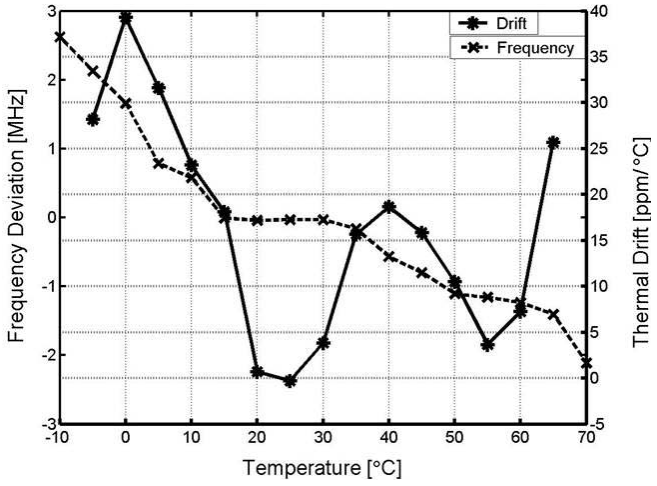

Fig.3. Frequency deviation (left axis) and thermal drift (right axis) of the VCO measured over a wide temperature range. The thermal frequency drift is approximately 0ppm/°C at room temperature and the frequency monotonically decreases as temperature increases.

The VCO was cycled from -10°C to +70°C in a temperature chamber at 5° increments and allowed to stabilize at each temperature step. The frequency at each step was measured and the results are shown in Fig. 3. At room temperature, the oscillator has a thermal frequency instability of approximately 0ppm/°C. The expected operating temperature range of the CSAC is 0°C to 50°C [9,10]. Over this range, the total frequency shift due to temperature is 2.9MHz, representing an average thermal drift of -17ppm/°C with a peak of -40ppm/°C at 0°C. The 3-MHz tuning range will compensate for this frequency change and increasing the value of the capacitor that loosely couples the varactor will increase this range if necessary at a small cost of phase noise.

IV. LOCKING TO THE ATOMIC RESONANCE

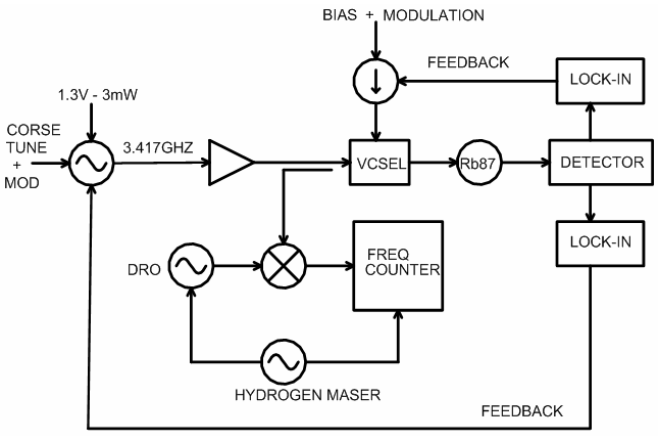

Fig.4. Schematic of the setup used at NIST to lock the VCO to the coherent population trapping (CPT) resonance of Rubidium atoms. The fractional frequency instability is measured as shown with a frequency counter referenced by the NIST hydrogen maser ensemble.

To demonstrate sufficient quality for application in chip-scale atomic clocks, the VCO has been locked to the CPT resonance of Rubidium atoms at the National Institute of Standards and Technology (NIST) in Boulder, CO. The setup is designed to mimic that used by future chip-scale atomic clocks. The diagram of the setup is shown in Fig. 4 and incorporates a laser (VCSEL) at the optical absorption frequency of Rubidium, an amplifier to recover power lost from attenuators and cables, a transparent cell containing gaseous Rb atoms, a photodetector, and the lock-in amplifiers necessary to adjust the VCSEL current and oscillator tune voltage. The inner schematic with the DRO, frequency counter, and maser is the setup used to measure the fractional frequency instability of the oscillator both when free-running and when locked to the resonance of the atoms (Fig. 5). In this measurement, a frequency-disciplined DRO is mixed with the RF output of the VCO and the beat frequency is measured by a frequency counter. The reference for the counter and the DRO is the NIST hydrogen maser ensemble, with far better stability than these measurements require.

The measured fractional frequency instabilities of the locked and unlocked oscillator are reported in Fig. 5. It is evident that the VCO has been locked to the atomic resonance by the large increase in stability, reaching a value of $6 \cdot 10^{-10}$ at approximately 200 seconds and is shown remaining in that vicinity up to one hour integration time. The DARPA

requirement for the chip-scale atomic clock is a fractional frequency instability of 10^{-11} at one hour integration time, which has obviously not been achieved here. However, such long-term stability is achieved primarily by the stability of the atoms, which is most likely the limitation in this measurement since this particular bench-top system was not optimized. It is understood that merely achieving a lock to this type of setup proves the viability of this VCO as a local oscillator for the chip-scale atomic clock.

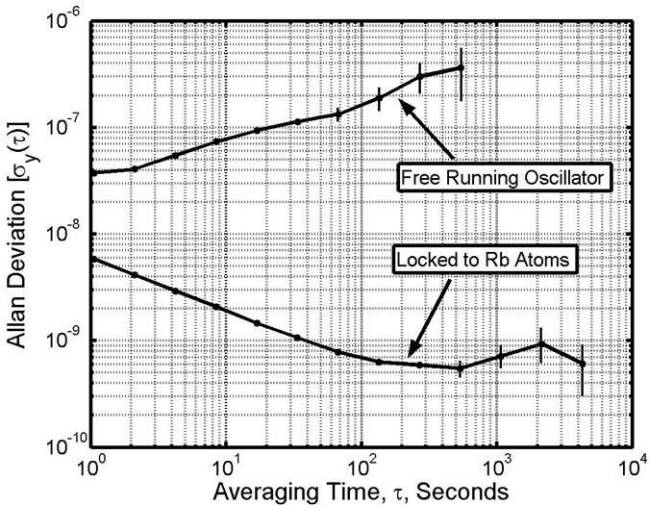

Fig.5. Fractional frequency instability of the free-running VCO (top) and when locked to Rubidium atoms at NIST (bottom). This shows the viability of this VCO for application in chip-scale clocks.

V. Conclusion

Prior to the design presented in this paper, it was considered that new and developing technologies like nanoelectromechanical resonators would be required to meet the local oscillator requirements for locking to the CPT resonance in chip-scale atomic clocks [3,13]. Recently fabricated FBAR resonators were also considered and may prove useful as the power consumption and thermal drift are reduced [14]. This paper demonstrates a low-power (2-mW) BJT micro-coaxial resonator oscillator at 3.417GHz that will meet all of the requirements in an inexpensive and reliable design. In summary, the oscillator is tunable over 3-MHz, with a phase noise of -33 dBc/Hz at 100Hz, and the size of the coplanar VCO is 0.49cm^2. The VCO was successfully locked to the CPT resonance of Rb atoms at NIST. The oscillator circuit is manufacturable using standard PCB surface-mount technology and the cost of all the parts does not exceed $8 in low quantities.

Acknowledgement

This work was supported in part by the U.S. Defense Advanced Research Projects Agency, under CSAC grant NBCH1020008.

Alan Brannon thanks the National Science Foundation for support from a Graduate Research Fellowship.

The authors express thanks to Dr. John Kitching, Dr. Peter Schwindt, and Vishal Shah from NIST for their successful efforts to lock our oscillator to their atomic physics setup.

The authors express thanks to Val Jackson of Val Jackson & Associates, Inc. for samples and technical advice on the coaxial ceramic resonators, and PicoSecond Pulse Labs in Boulder, CO, for use of the temperature chamber.

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