Linearity of X-Band Class-E Power Amplifiers in EER Operation

Narisi Wang, *Student Member, IEEE*, Xinli Peng, *Student Member, IEEE*, Vahid Yousefzadeh, *Student Member, IEEE*, Dragan Maksimović, *Member, IEEE*, Srdjan Pajić, *Student Member, IEEE*, and Zoya Popović, *Fellow, IEEE*

***Abstract*—Multifunctional RF front ends need to transmit different types of signals while maintaining efficiency and signal quality. This paper addresses efficient transmitter power amplifiers (PAs) for signals with varying peak-to-average ratios, requiring simultaneous efficiency and linearity. Linearity characterization of class-E high-efficiency PAs operating in envelope elimination and restoration (EER) mode is discussed. Specifically, a 67%-efficient 10-GHz MESFET PA is characterized in terms of its AM–AM, AM–PM conversion and intermodulation products. Measurements of intermodulation distortion are compared with harmonic-balance simulations using TriQuint's Own Model provided by the device manufacturer. It is shown experimentally and through simulations that the amplifier in the EER mode has improved linearity while maintaining high-efficiency operation.**

***Index Terms*—Class-E, efficiency, envelope elimination and restoration (EER), linearity, power amplifier (PA).**

I. Introduction

HIGH-EFFICIENCY class-E power amplifiers (PAs) can accomplish ultrahigh efficiencies by driving the transistor as a switch [1], [2]. For an ideal class-E PA, the efficiency is 100% [1], [3]–[5] and, in practice, it is limited by the on resistance of the active device and the maximum current and voltage handling capabilities. Since the transistor is driven into deep saturation, these amplifiers exhibit high nonlinearities and are not useful for some types of signal modulations [6]. For multifunctional systems where power is the prime resource, a high-efficiency transmitter with linearity that adapts to the input signal type has the potential of significant power savings over time. This paper presents systematic nonlinearity characterization of X-band class-E PAs with the goal of using adaptive fast and slow bias control for improving linearity.

PAs with dynamic bias for efficiency improvement have been presented in [7]–[9]. Efficiency improvements of a 950-MHz MESFET PA with a boost dc–dc converter modulator [7] and a 835-MHz PA with a class-S modulator [8] have been demonstrated. In [9], a detector at the output of a 67%-efficient 20.3-dBm class-E PA provides a feedback signal to the drain bias controller implemented with a 96% efficient Buck dc–dc converter. Compared with a PA with constant drain bias (4 V), the average efficiency for a uniform power probability distribution is improved by a factor of 1.4 over an output power between 15–20 dBm. The efficiency improves from 22% to 65% at the lower power levels.

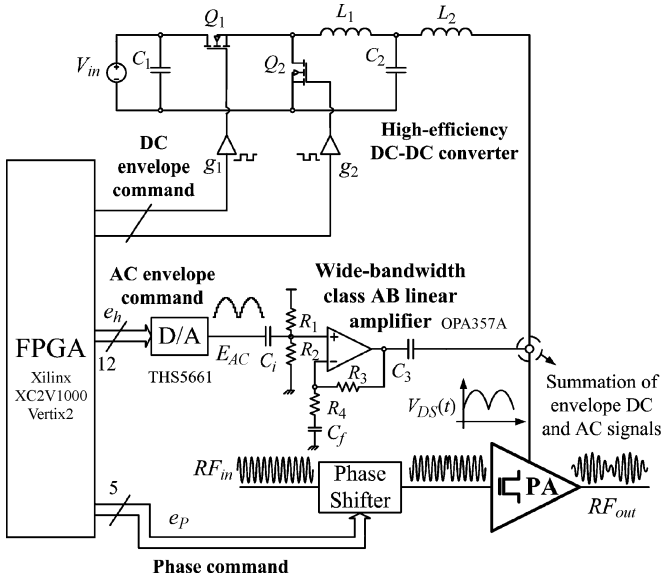


Fig. 1. Block diagram of the EER system with FPGA bias control. The RF PA is a class-E 10-GHz MESFET amplifier. The envelope signal is split into a dc component, which controls the dc–dc synchronous Buck converter and an ac component, which provides envelope ac variations. The phase of the signal provides control of the phase of the carrier input to the PA through an X-band digitally controlled phase shifter.

Dynamic biasing can be used not only for efficiency improvement, but also for linearization of highly saturated efficient PAs, such as in the envelope elimination and restoration (EER) technique, in which the amplitude and phase information of the input signal are separated [10]. The drive contains only phase information with a constant amplitude, while the amplitude information is provided through the bias, thus restoring the envelope information at the output.

In this paper, the linearity study of a 10-GHz class-E PA in EER operation is presented as follows.

- Section II presents background on EER and discusses the implementation of the EER transmitter, as shown in Fig. 1. The individual components are discussed in detail: the class-E 10-GHz PA; fast dynamic bias control circuitry; and the digital control signal generation using a field-programmable gate array (FPGA).

Manuscript received April 22, 2004; revised November 2, 2004. This work was supported by the Defense Advanced Research Projects Agency under the Intelligent RF Front Ends Program, under Grant N00014-02-1-0501, and by Wyle Laboratories, Wright-Patterson Air Force Base under Grant PO 19035.0D.31-369S.

N. Wang, V. Yousefzadeh, D. Maksimović, S. Pajić, and Z. Popović are with the Department of Electrical and Computer Engineering, University of Colorado at Boulder, Boulder, CO 80302 USA.

X. Peng is with Maxim Integrated Products, Chandler, AZ 85003 USA.

Digital Object Identifier 10.1109/TMTT.2005.843500

- Section III discusses linearity (AM–AM and AM–PM) of an X-band class-E PA with a continuous wave (CW) single-frequency input signal.
- Section IV presents two-tone test results for the narrow-band X-band PA with and without bias control.
- Section V is a discussion of linearity over a range of frequencies within X-band.

II. High-Efficiency X-Band EER Transmitter

A number of authors have demonstrated EER transmitters at lower frequencies, e.g., an EER transmitter for HF/VHF is demonstrated in [11] where a class-D PA at 3.5 MHz with a class-S modulator is used. The system efficiency is approximately 60% and a two-tone third-order intermodulation distortion (IMD3) of better than −40 dBc is achieved with the envelope detector as a major source of nonlinearity. In [12], the effect of envelope modulator bandwidth and time delay between the envelope and phase signal on the linearity is studied theoretically. An attempt to limit the feedthrough, another cause of nonlinearity, by modulating the input signal drive, is shown in [13], while [14] theoretically analyzes the effect of load network and RF choke on the linearity.

Limited work has been done in EER at microwave frequencies. For example, in [6], the efficiency and linearity behavior of a 8.4-GHz class-F PA is studied for both general linear mode (with constant biasing) and EER mode for different manually controlled drain bias schemes. An IMD3 ratio of −27 dBc with a time-average efficiency for a multi-carrier signal with 10-dB peak-to-average ratio of 44% is obtained for a modified EER mode. This is a factor of 4.4 improvement over a 10% efficient backed-off class-A PA with the same IMD3 ratio using the same device.

In this paper, we demonstrate a full implementation of an X-band transmitter (Fig. 1). Efficient wide-band envelope tracking, which is required in the EER scheme, is achieved through a combination of a switched-mode power converter and a linear class-AB amplifier (OPA357A). Similar combined switching/linear amplifiers have been reported for audio applications [15] and for EER transmitters [16], [17]. The digital PA system controller is constructed using a Xilinx Virtex-II V2MB1000 FPGA. The system controller allows the flexibility of generating arbitrary lookup-table-based periodic envelope and phase waveforms for testing the PA. In this test setup, we have not considered generation of arbitrary complex modulation signals. The dc portion of the envelope signal is provided through an efficient synchronous Buck dc–dc switching converter. The remainder of this section provides details of the components of Fig. 1.

A. Class-E PA

The class-E PA is similar to the design presented in [2] and [9]. The active device is a general-purpose GaAs MESFET AFM04P2-000 from Alpha Industries Inc., Woburn, MA. For the transistor with known output capacitance $C_{\rm OUT}$, determined initially from small-signal S-parameters, the optimal class-E load impedance for 50% duty cycle can be calculated as [1], [18]

$$Z_E = \frac{0.28}{C_{\rm OUT}\cdot\omega} e^{j49^\circ}. \tag{1}$$

The output capacitance of the MESFET AFM04P2-000 is determined to be $C_{\rm OUT} = 0.11$ pF. Using (1), the optimal class-E load impedance at 10 GHz is $Z_E = R_E + jX_E \approx 27 + j31\,\Omega$. Ideal class-E operation requires high-impedance termination of all higher harmonics. However, it is empirically determined that termination of only the second harmonic gives a reasonable approximation of the ideal class-E mode [2]. On the input side, matching for maximal power transfer is performed, using given S-parameters of the active device. The active device has a maximum drain-to-source voltage of 6 V and the maximum drain current of 140 mA. It is capable of delivering 21 dBm of output power with gain of 9 dB while operating in 1-dB compression at 18 GHz. The layout of the class-E amplifier is shown in Fig. 2. Output matching is provided using a single open shunt stub, and the second harmonic termination is performed using another open shunt stub, with electrical length of 90° at the second harmonic frequency (20 GHz). DC gate and drain bias voltages are provided through high-impedance quarter-wavelength bias lines, and dc decoupled from the source and load using 8.2-pF millimeter-wave capacitors.

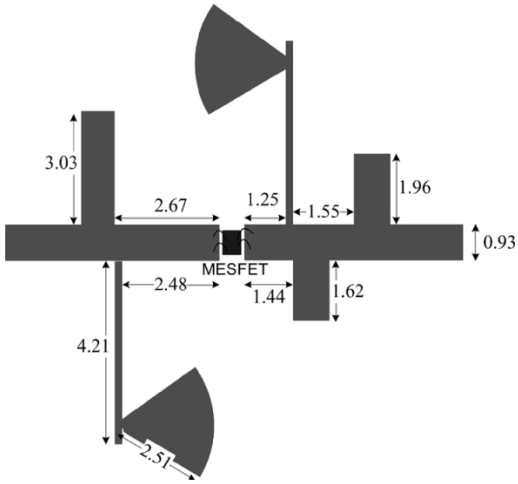


Fig. 2. Layout of the class-E amplifier. The substrate is Rogers TMM6 with $\epsilon_r = 6$ and a thickness of 0.635 mm. The active device is a GaAs MESFET AFM04P2-000 from Alpha Industries Inc. All units are given in millimeters.

Due to numerous nonidealities such as: 1) finite ON resistance; 2) finite switching speed; 3) drain–voltage dependent output capacitance; 4) device parasitics (pad inductances and capacitances, bond-wire inductances, etc.); and 5) mounting parasitics, the analytically calculated class-E load impedance does not give optimal performance. However, (1) is an excellent starting point for either a nonlinear computer-aided design (CAD) design or a load–pull-based design. For an input power of 13 dBm, a summary of PA characteristics is as follows.

- Saturated gain $G = 6.5$ dB at $P_{\rm out} = 19.5$ dBm.
- Drain efficiency $\eta = 67\%$ at $P_{\rm out} = 19.5$ dBm.
- Power-added efficiency $PAE = 52\%$ at $P_{\rm out} = 19.5$ dBm.

The class-E switched mode amplifier naturally lends itself to EER. This can be seen by considering the output circuit of an ideal class-E amplifier, which consists of an ideal switch in parallel with the output capacitance of the active device connected to the load through a matching network. From the derivation in [18], the open switch voltage can be written as

$$v_{\rm open}(t) = \frac{I_{DD}}{C_{\rm OUT}\cdot\omega}\Big[\omega t - a\big(\cos(\omega t-\phi)-\cos(\phi)\big)\Big] \quad (2)$$

where $a = 1.86$ and $\phi = 32.48°$. The switch voltage is zero during the other half cycle. I_{DD} is the dc drain supply current and ω is the operating (switching) angular frequency. If the dc supply is provided through an ideal RF choke, the average value of the switch voltage is equal to the supply voltage V_{DD}

$$V_{DD} = \frac{1}{T}\int_0^{\frac{T}{2}} v_{\rm open}(t)\cdot dt = \frac{I_{DD}}{\pi\omega C_{\rm OUT}}. \quad (3)$$

In an ideal class-E mode, the harmonics are perfectly terminated, thus, the power delivered to the output matching network is

$$P_{\rm OUT} = \frac{R_E}{2}(1.86\pi\omega C_{\rm OUT})^2\cdot V_{DD}^2. \quad (4)$$

Since $P_{\rm OUT} = V_{\rm OUT}^2/(2\cdot R_L)$, in a class-E amplifier, the output voltage across the load R_L is linearly proportional to the drain bias voltage. This, in turn, means that control of the drain bias according to the envelope of the input signal accomplishes envelope amplification.

B. High-Efficiency DC–DC Converter and Fast Bias Control

The power switches Q_1 and Q_2 in the dc–dc converter are controlled by the complementary gate-drive signals g_1 and g_2 generated by the FPGA controller [19]. The duty cycle of Q_1 adjusts the dc value of the envelope signal. The ac portion $E_{\rm AC}$ of the envelope signal is generated by the FPGA through the THS5661 12-bit 100 megasamples/s (MSPS) DAC. The ac portion is then buffered and amplified by a wide-band class-AB amplifier, constructed around the OPA357 op-amp. The dc and ac signals are coupled through the inductor L_2 and capacitor C_3 to obtain the supply voltage $V_{\rm DS}(t)$ for the class-E PA. The phase of the RF input signal for the PA is controlled by a TriQuint TGP6336-EEU 5-bit X-band digitally controlled phase shifter. The phase shifter has around 9-dB loss, requiring a pre-amplifier at the input (not shown for clarity). The digital phase command e_P is also generated by the FPGA controller.

C. Digital Signal Generation and Control

The digital system controller for the dc–dc converter is described in detail in [19]. Fig. 3 shows the block diagram of the part of the digital controller responsible for generation of the digital ac envelope command e_h, and the digital phase command e_P. For the standard two-tone test signal, the envelope command is a rectified sinusoidal signal. The ac portion of the rectified sinusoidal signal is implemented in a lookup table on

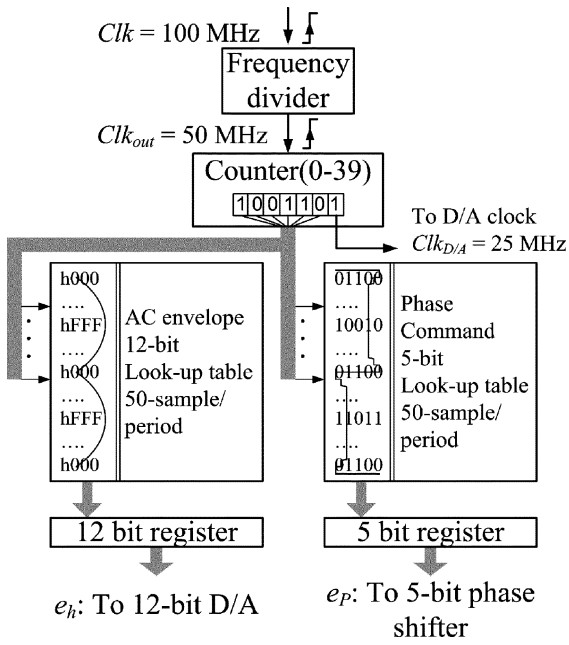


Fig. 3. Digital controller block diagram of the ac envelope command e_h and phase command e_p.

the FPGA. There are 50 samples per period of the equivalent sinusoidal waveform (or 25 samples per period of the rectified sinusoid). Since the rectified sine wave has significant harmonic components, the relatively high oversampling rate (25 times the period) is necessary in the PA test setup. Each sample is 12-bit long. A counter selects the samples of the rectified sinusoid from the lookup table at a frequency of 25 MHz. The sample values are registered in a 12-bit register, which is the digital command e_h for the 12-bit DAC. A 25-MHz clock is generated for the DAC, which reads the 12-bit registered value e_h of the sampled signal. In this implementation, the frequency of the rectified sinusoid is $f_{eh} = 2\times(25\ \text{MHz})/(50\ \text{samples}) = 1$ MHz. The 25-MHz sample frequency is generated from the 100-MHz internal clock of the FPGA. The maximum FPGA clock frequency of 100 MHz, and the need for a relatively high sampling rate limit the maximum frequency of the generated envelope signal to 1 MHz. By increasing the number of samples per period in the lookup table or by modifying the frequency divider, lower frequencies of the envelope signal can be easily achieved.

The second lookup table shown in Fig. 3 provides the 5-bit phase command e_P for the phase shifter. Corresponding to the 50 samples per period of the equivalent sinusoidal waveform amplitude, there are 50 samples recorded in the phase lookup table. The same counter that selects the sample value of the rectified sinusoid is used to provide the phase data samples. As a result, the phase and the ac envelope signals are synchronized. By shifting the phase or envelope data up or down in the lookup table, the delay between the envelope and phase command signals can be controlled in order to compensate for the delay in the envelope and phase signal paths. Given the 25-MHz sample-clock frequency, the resolution for the delay compensation is 40 ns. Measured envelope and phase signals generated using the scheme in Fig. 3, for the two-tone test to be described later, are shown in Fig. 4.

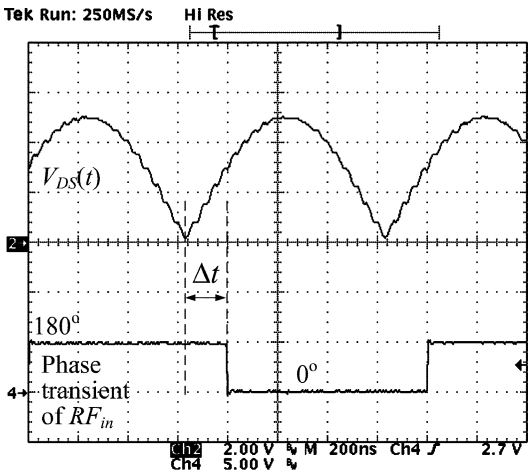


Fig. 4. Generated drain bias and phase of the input RF signal for two-tone test of the PA in EER mode. Δt is the time delay between the two signal.

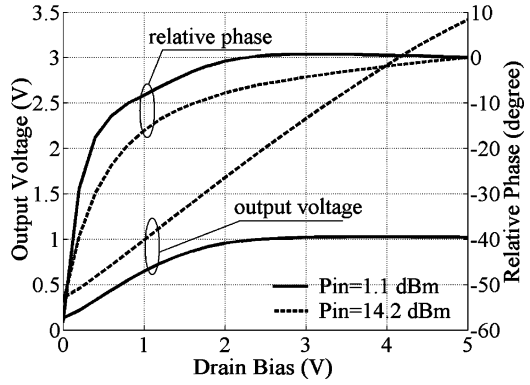


Fig. 5. Measured AM–AM and AM–PM characteristics of the class-E PA with the amplitude modulation through the drain bias. The solid line is the result for a low (1.1 dBm) input signal, while the dashed line corresponds to a high input power level of 14.2 dBm when the output power is the maximum 20.6 dBm.

III. Narrow-Band Linearity Characterization of the PA

The linearity of the class-E PA is characterized by considering the drain bias as the input signal amplitude. In this context, the AM–AM conversion is measured as the increase in output voltage (output power into a 50-Ω load) when the drain bias is increased linearly. When the drain bias is 5 V, the small-signal gain of the PA in general linear mode is approximately 9 dB at an input power of 1.1 dBm, and saturates at 6.5 dB for the high input power of 14.2 dBm. For high input power, the PA output voltage varies linearly with drain bias, as shown in Fig. 5. Class-E PAs are designed to operate with high input power, and when the input power is reduced, the PA AM–AM characteristics are no longer linear, as shown in solid line in Fig. 5. This is consistent with the approach shown in Fig. 1 where the level of the input signal to the PA is kept at a constant high level. Another feature in Fig. 5 is existence of an output voltage with zero drain bias, referred to as feedthrough, which introduces distortion in signals that have envelope zero crossings.

For AM–PM conversion, the relative phase between input and output signals of the PA is measured for a linearly increasing drain bias, and the results are given for a high- and low-input power level. The class-E PA shows considerable AM–PM conversion for low levels of drain bias, again introducing distortion for signals with envelope zero-crossings.

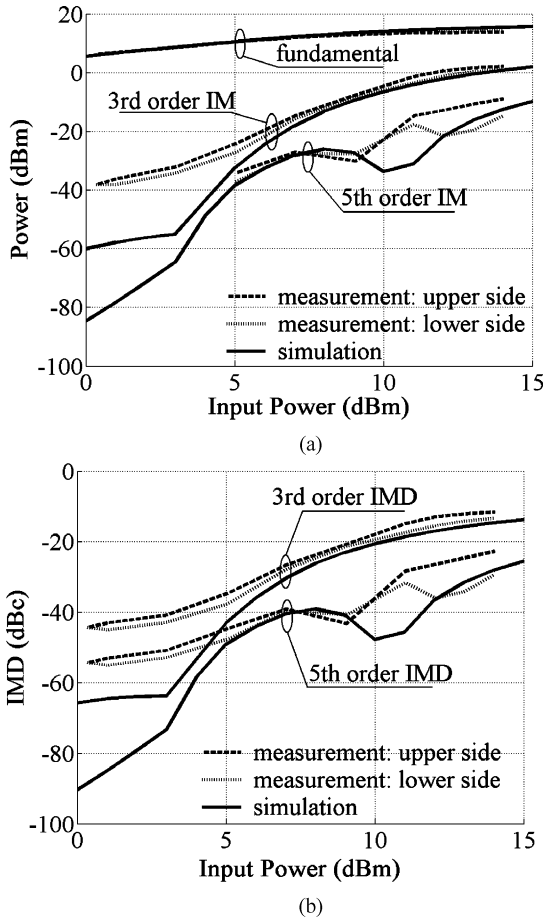


Fig. 6. Measured and simulated two-tone test of the class-E PA. (a) Fundamental and intermodulation product power levels as a function of input power. (b) IMD3 and IMD5 as a function of input power. The "upper and lower side" labels refer to the sidebands produced by the two-tone test.

IV. Two-Tone Characterization of PA in General Linear Mode

Another important measure of linearity, intermodulation distortion, is usually measured using a two-tone test [20]. We present two types of two-tone measurements for frequency spacing of 1 MHz: standard measurement for the PA at a constant drain bias of 4.2 V with two-tone test signals at 9.9995 and 10.0005 GHz, and a two-tone test for the PA in EER mode.

The measurements are compared to nonlinear harmonic-balance Agilent ADS simulations with TriQuint's Own Model (TOM) nonlinear model [21] for the MESFET (provided by the manufacturer).

Fig. 6 shows the level of intermodulation product versus input power at a drain bias of 4.2 V. As expected, the class-E PA has poor linearity: at an input power of 14 dBm, the IMD3 is around −10 dBc, while the fifth-order intermodulation product (IMD5) is approximately −25 dBc. This figure also shows an asymmetry in the upper and lower intermodulation sideband, commonly observed in RF PAs and attributed to memory effects [20].

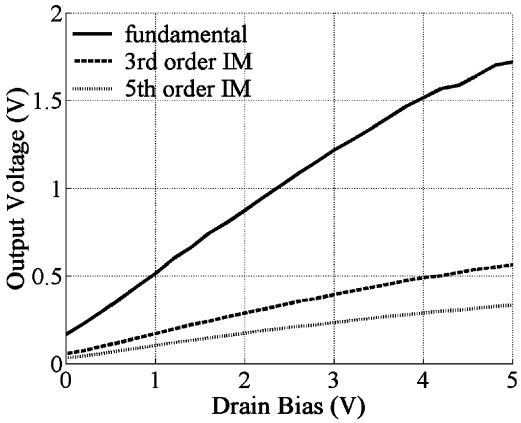


Fig. 7. Measured intermodulation product level as a function of drain bias for a phase-modulated input signal. The output voltage is calculated from the measured power across a 50-Ω load. Input power level is 13 dBm.

A. Two-Tone Dynamically Biased PA Characterization

In a two-tone test ($f_2 > f_1$), the input signal can be written as

$$v(t) = V\cos(2\pi f_1 t) + V\cos(2\pi f_2 t) \tag{5}$$

which becomes

$$\begin{aligned} v(t) &= 2V\left|\cos\left(2\pi\frac{f_2 - f_1}{2}t\right)\right|\cos\left[2\pi\frac{f_1 + f_2}{2}t + \phi(t)\right] \\ &= A(t)\cos\left[2\pi f_c t + \phi(t)\right] \end{aligned} \tag{6}$$

where f_c is the center carrier frequency, $A(t)$ is the amplitude which varies at a frequency of $(f_2 - f_1)$, and $\phi(t)$ alternates from 0 to π at half the frequency. Referring to the measurement setup in Fig. 1, $A(t)$ and $\phi(t)$ are controlled by the envelope command signal e_h and the phase command signal e_P. $A(t)$ becomes the drain bias voltage $V_{\rm DS}(t)$, which is shown in Fig. 4 along with the phase of the input RF signal. When the relative time delay between those two signals changes between $\Delta t = 0$ and $\Delta t = 1/[2(f_2 - f_1)]$, the alignment of the waveforms in the time domain changes from synchronous to asynchronous. We refer to these conditions as "in-phase" and "out-of-phase," respectively. In the experiments presented here, $f_c = 10$ GHz and $f_2 - f_1 = 1$ MHz.

Fig. 7 shows the measured bias dependence of the fundamental frequency output voltage, as well as the voltage of the third and fifth intermodulation products for a phase-modulated signal, which can be expressed as $\cos[2\pi f_c t + \phi(t)]$. All three voltages are approximately linearly dependent on the drain bias. This indicates that the EER mode of operation can linearize the PA.

Fig. 8 shows the measured power of the fundamental and the third and fifth intermodulation products as a function of input power to the PA for $\Delta t = 0$ (in-phase) and $\Delta t = 1/[2(f_2 - f_1)]$ (out-of-phase), respectively. The two sets of curves (solid and dashed lines) correspond to the upper and lower sidebands. As expected, the in-phase case shows a slower increase in intermodulation product power as the input power increases. The IMD3 and IMD5 for $\Delta t = 0$ (in-phase) and $\Delta t = 1/[2(f_2 - f_1)]$ (out-of-phase) are presented in Fig. 9(a) and (b), respectively, and summarized as follows.

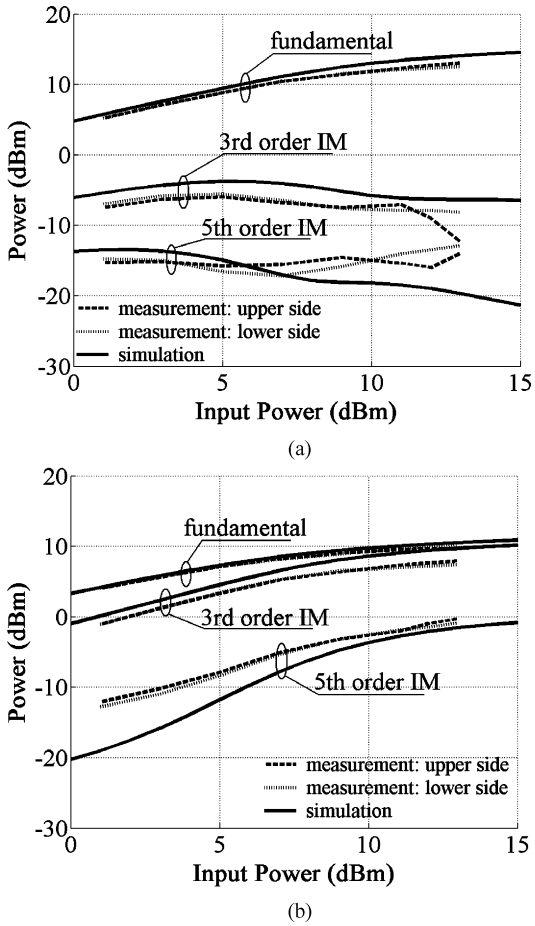


Fig. 8. Measured power of the fundamental and the third and fifth intermodulation products as a function of input power to the PA. (a) $\Delta t = 0$ (in-phase). (b) $\Delta t = 1/[2(f_2 - f_1)]$ (out-of-phase). The three sets of curves correspond to the upper and lower sidebands and simulation results.

- For the in-phase case, the measured IMD3 and IMD5 are -20 and -25 dBc (around input power level of 13 dBm), respectively, where ideally no intermodulation products should be present.
- For the out-of-phase case the measured IMD3 and IMD5 are -3 dBc and -11 dBc (around input power level of 13 dBm), respectively. The calculated theoretical results (ideal class-E) are IMD3 of 0 dBc and IMD5 of -9.5 dBc. The reason for the difference is attributed to nonlinearity caused by AM–PM and feedthrough when the drain bias is zero.
- Harmonic-balance simulations of the IMD levels agree well with the measurements.
- For the in-phase case, with input power increase, the IMD level decreases due to the dynamic biasing. This can also be understood by observing the results in Fig. 5.

V. Frequency Response of PA in EER Mode

The results discussed are for single-frequency or narrow-band operation. It is of interest to examine the behavior of the class-E

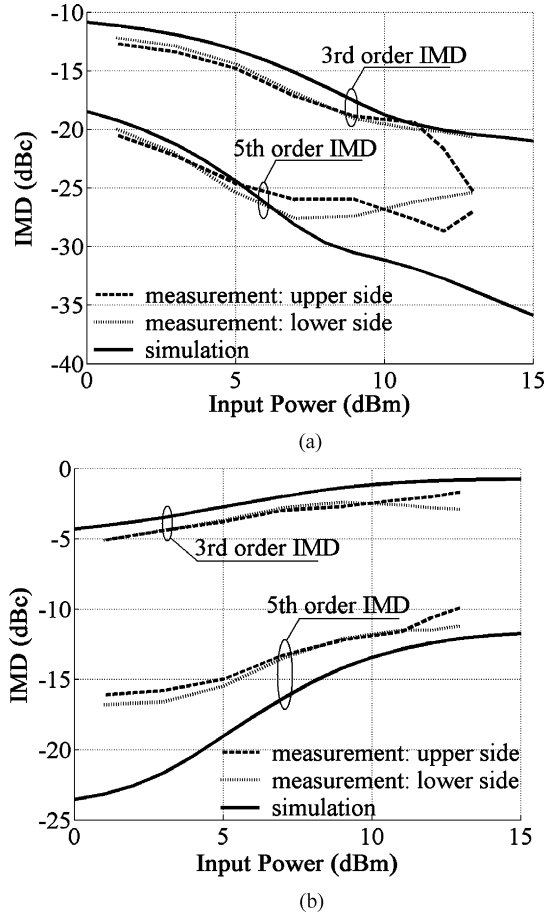


Fig. 9. IMD3 and IMD5 for: (a) $\Delta t = 0$ (in-phase) and (b) $\Delta t = 1/[2(f_2 - f_1)]$ (out-of-phase). The three sets of curves correspond to the upper and lower sidebands and simulation results.

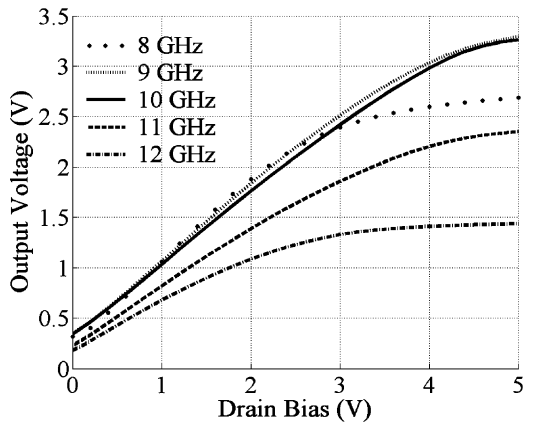


Fig. 10. Measured output voltage (50-Ω load) as a function of drain bias (AM–AM) for different frequencies around the 10-GHz design frequency. Input power level is 13 dBm.

EER mode over a range of frequencies around the class-E design frequency. The AM–AM of the class-E PA in EER mode, i.e., output voltage versus the drain bias, is measured from 8 to 12 GHz. Fig. 10 shows the output voltage versus drain bias for five different frequencies. When the frequency deviates from 10 GHz, the PA class of operation changes, resulting in degraded linearity. Typical class-E mode bandwidth is on the order

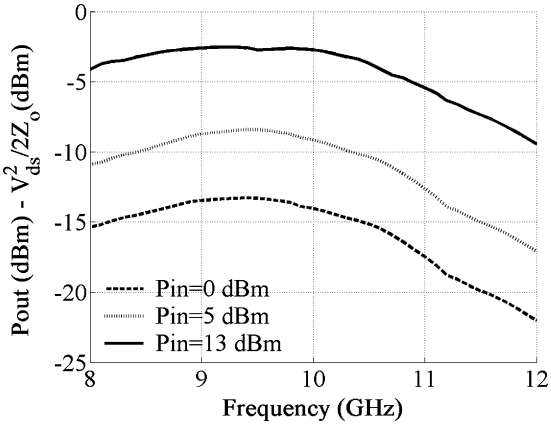


Fig. 11. Frequency dependence of the quantity $P_{\rm out}/(V_{\rm ds}^2/2Z_o)$, which represent the ratio of the RF output power to the bias voltage across a 50-Ω load.

of 10% (e.g., [2]) and is limited by the output matching network that provides harmonic termination and the optimal fundamental load for high-efficiency operation. Fig. 11 shows the frequency dependence of the quantity $P_{\rm out}/(V_{\rm ds}^2/2Z_o)$, which represents the ratio of the RF output power to the bias voltage across a 50-Ω load. In this way, a 1-dB bandwidth for EER mode can be defined and is measured to be around 24% (8.1–10.5 GHz).

VI. Conclusion

In summary, this paper has presented linearity characterization of highly saturated high-efficiency class-E X-band PAs. It has been shown both experimentally and in simulations that the EER mode with dynamic biasing of the PA can improve linearity significantly. Harmonic-balance simulations have been shown to be useful for design that includes linearity considerations. The results in this paper have demonstrated the possibility of more generally adaptive PAs. Any input signal can be presented in baseband in polar instead of I/Q form, allowing nonlinear PAs to be used when linearity is a requirement. In addition, the FPGA in Fig. 1 can be used for basedband predistortion. The dynamic biasing circuit bandwidth needs to exceed the signal bandwidth, and digitally controlled high-speed power management circuits are a topic of continued research.

Acknowledgment

The authors thank Dr. D. Purdy, Office of Naval Research (ONR), Washington, DC, and Dr. P. Watson, Wright-Patterson Air Force Base (WPAFB), Dayton, OH, for helpful comments.

References

[1] T. B. Mader and Z. B. Popović, "The transmission-line high-efficiency class-E amplifier," *IEEE Microw. Guided Wave Lett.*, vol. 5, no. 9, pp. 290–292, Sep. 1995.

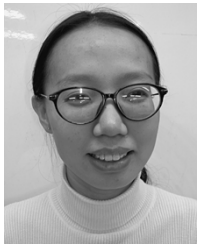
[2] S. Pajić and Z. Popović, "An efficient X-band 16-element spatial combiner of switched-mode power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 7, pp. 1863–1870, Jul. 2003.

[3] A. D. Artym, "Switching mode of high frequency power amplifiers," *Radiotekhnika Mosk.*, vol. 24, Jun. 1969.

[4] N. O. Sokal and A. D. Sokal, "Class-E—A new class of high efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-10, no. 6, pp. 168–176, Jun. 1975.

[5] F. H. Raab, "Idealized operation of the class-E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-24, no. 12, pp. 725–735, Dec. 1977.

[6] M. Weiss, F. Raab, and Z. Popović, "Linearity of X-band class-F power amplifiers in high-efficiency transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1174–1179, Jun. 2001.
[7] G. Hanington, P. Chen, P. Asbeck, and L. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.
[8] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R. Sherman, and T. Quach, "High efficiency CDMA RF power amplifier using dynamic envelope tracking technique," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2000, pp. 873–876.
[9] N. Wang, V. Youzefzadeh, D. Maksimović, S. Pajić, and Z. Popović, "60% efficient 10-GHz power amplifier with dynamic drain bias control," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 3, pp. 1077–1081, Mar. 2004.
[10] L. Kahn, "Single sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, no. 7, pp. 803–806, Jul. 1952.
[11] F. H. Raab and D. J. Rupp, "High-efficiency single-sideband HF/VHF transmitter based upon envelope elimination and restoration," in *Proc. 6th Int. HF Radio Systems Techniques Conf.*, Jul. 1994, pp. 21–25.
[12] F. H. Raab, "Intermodulation distortion in Kahn-technique transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 12, pp. 2273–2278, Dec. 1996.
[13] ——, "Drive modulation in Kahn-technique transmitters," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1999, pp. 811–814.
[14] M. Kazimierczuk, "Collector amplitude modulation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-31, no. 6, pp. 543–549, Jun. 1984.
[15] R. van der Zee and E. van Tuijl, "A power-efficient audio amplifier combining switching and linear techniques," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 985–991, Jul. 1999.
[16] P. Midya, "Linear switcher combination with novel feedback," in *IEEE Power Electronics Specialists Conf.*, vol. 3, Jun. 2000, pp. 1425–1429.
[17] F. H. Raab, P. Azbeck, S. Cripps, P. B. Kenington, Z. B. Popović, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.
[18] T. B. Mader, E. W. Bryerton, M. Marković, M. Forman, and Z. Popović, "Switched-mode high-efficiency microwave power amplifiers in a free-space power-combiner array," *IEEE Trans. Microw. Theory Tech.*, pt. 1, vol. 46, no. 10, pp. 1391–1389, Oct. 1998.
[19] V. Yousefzadeh, N. Wang, D. Maksimović, and Z. Popović, "Digitally controlled DC–DC converter for RF power amplifier," in *IEEE Applied Power Electronics Conf. Exp.*, vol. 1, 2004, pp. 81–87.
[20] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*. Norwood, MA: Artech House, 2002, pp. 73–110.
[21] A. McCamant, G. McCormack, and D. Smith, "An improved GaAs MESFET model for SPICE," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 6, pp. 822–824, Jun. 1990.



Narisi Wang (S'00) received the B.S. degree in electrical engineering from the Beijing University of Posts and Telecoms, Beijing, China, in 1999, the M.S. degree in electrical engineering from Colorado State University, Fort Collins, in 2001, and is currently working toward the Ph.D. degree at the University of Colorado at Boulder. Her master's research concerned mathematical modeling of coaxial probe crack detection. Her doctoral research concerns microwave PAs.

Xinli Peng (S'01) received the M.S. degree in electrical engineering from the University of Colorado at Boulder, in 2002.

He is currently an Integrated Circuit (IC) Design Engineer with Maxim Integrated Products, Chandler, AZ, where he is involved with power management IC design for portable equipment. His previous research has included high-power RF semiconductor devices, power electronics, and analog IC design.

Vahid Yousefzadeh (S'03) received the B.S. degree in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 1994, and is currently working toward the Ph.D. degree at the University of Colorado at Boulder.

From 1994 to 2002, he was an Electrical Engineer for the Namvaran Engineering Company and the Bina_Afzar Research Company. His current research concerns power management for RF PAs.

Dragan Maksimović (M'89) received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, Belgrade, Yugoslavia, in 1984 and 1986, respectively, and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1989.

From 1989 to 1992, he was with the University of Belgrade. Since 1992 he has been with the Department of Electrical and Computer Engineering, University of Colorado at Boulder, where he is currently an Associate Professor and Co-Director of the Colorado Power Electronics Center (CoPEC). His current research interests include power electronics for low-power portable systems, digital control techniques, and mixed-signal IC design for power-management applications.

Dr. Maksimović was the recipient of the 1997 National Science Foundation (NSF) CAREER Award, and a Power Electronics Society Transactions Prize Paper Award.

Srdjan Pajić (S'02) received the Dipl. Ing. degree from the University of Belgrade, Belgrade, Yugoslavia, in 1995, the M.S. degree from the University of Colorado at Boulder, in 2002, and is currently working toward the Ph.D. degree in electrical engineering at the University of Colorado at Boulder.

From 1995 to 2000, he was a Research and Design Engineer with IMTEL Microwaves, Belgrade, Yugoslavia, where he was involved with the development of PAs for radio and television broadcast systems. In 2002 he received a M.S. at the University of Colorado at Boulder. His research interests include high-efficiency microwave PAs for active antennas, linear PAs for wireless communications, and quasi-optic power-combining techniques.

Zoya Popović (S'86–M'90–SM'99–F'02) received the Dipl. Ing. degree from the University of Belgrade, Yugoslavia, in 1985, and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1990.

Since 1990, she has been with the University of Colorado at Boulder, where she is currently a Full Professor. She has developed five undergraduate and graduate electromagnetics and microwave laboratory courses and coauthored (with her father) the textbook *Introductory Electromagnetics* (Upper Saddle River, NJ: Prentice-Hall, 2000) for a junior-level core course for electrical and computer engineering students. Her research interests include microwave and millimeter-wave quasi-optical techniques, high-efficiency microwave circuits, smart and multibeam antenna arrays, intelligent RF front ends, RF optical techniques, batteryless sensors, and broad-band antenna arrays for radio astronomy.

Dr. Popović was the recipient of the 1993 Microwave Prize presented by the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) for the best journal paper. She was the recipient of the 1996 URSI Isaac Koga Gold Medal. In 1997, Eta Kappa Nu students chose her as a Professor of the Year. She was the recipient of a 2000 Humboldt Research Award for Senior U.S. Scientists from the German Alexander von Humboldt Stiftung. She was also the recipient of the 2001 Hewlett-Packard (HP)/American Society for Engineering Education (ASEE) Terman Award for combined teaching and research excellence.