A Digitally Controlled DC/DC Converter for an RF Power Amplifier

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***Abstract*—This paper describes design and implementation of a digitally controlled dc/dc converter that provides a dynamically adjustable supply voltage for a radio frequency power amplifier (RFPA). The techniques employed in the design include a combination of constant-frequency continuous conduction mode (CCM) and a variable-frequency discontinuous conduction mode to achieve very high converter efficiency over a wide range of output power levels. The variable-frequency converter control is accomplished using a current-estimator circuit, which eliminates the need for current sensing. A field-programmable gate array (FPGA)-based digital controller implementation allows programmability of the mode transition and other controller parameters. In the complete experimental system, which consists of the digitally controlled dc/dc converter and a class-E RFPA operating at 10 GHz, experimental results show that the overall system efficiency is significantly improved over a wide range of RFPA output power levels.**

***Index Terms*—Radio frequency power amplifier (RFPA).**

I. Introduction

In battery-operated wireless systems, such as mobile phones, a radio frequency power amplifier (RFPA) is often the most significant power-consuming component. To minimize the power consumption, a system-level power management scheme adjusts the RFPA output power over a wide range. With a fixed drain supply voltage, the RFPA efficiency at lower power levels is very low, which adversely affects the average power consumption and the battery life. To improve the RFPA efficiency over the wide range of power, dynamic control of the drain supply voltage has been proposed [1]–[6]. The technique of adjusting the RFPA supply voltage in accordance with an output RF power command is now supported by dedicated switched-mode power supply integrated circuits, such as [7], [8].

In this paper, we present a closed-loop implementation of the RFPA power control through the drain supply voltage. The objectives are to improve the RFPA system efficiency and enable precise control over a range of output power levels using an efficient dc/dc converter in the control loop. It should be noted that in this application the dc/dc converter is not required to follow a fast-varying envelope of the RF signal. Instead, the purpose of the dc/dc converter in the slow power control loop is to efficiently generate the dc drain supply voltage necessary to produce the desired output RF power level. This system is suitable for constant-envelope RF signals.

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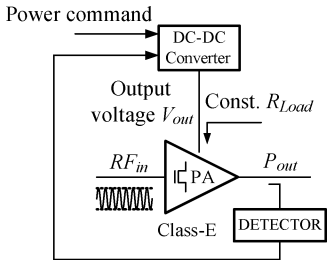

Fig. 1. System block diagram: RF power amplifier (RFPA) is supplied from a dc/dc converter. The converter and the RFPA form a closed-loop power control system where the supply voltage $V_{\rm out}$ to the RFPA is adjusted so that the sensed RF output power matches the power command.

A system block diagram implementing the closed-loop RF power control through the drain supply voltage is shown in Fig. 1. In this system, the RFPA is a high-efficiency X-band class-E amplifier [4]. The output RF power is sensed through a detector and compared to a power command signal. In response to the error between the sensed RF power and the command power, the dc/dc converter adjusts the output voltage. In steady state, the measured output power ideally equals the power command. The system specifications allow the switching frequency ripple of about 20 mV, and the power control bandwidth of about 10 kHz. The output RF power is in the range from 5 to 20 dBm. Compared to a more traditional realization where the drain supply voltage for the RFPA is constant, the overall efficiency improvement depends on the dc/dc converter which should be capable of maintaining very high efficiency over a wide range of output voltages and output power levels.

This paper describes design and implementation of a digitally controlled buck dc/dc converter that takes into account the RFPA requirements. Efficiency optimization over the wide range of power is addressed through two different modes of operation: zero-voltage-switching constant-frequency continuous conduction mode (CCM) is applied at higher power levels; pulse frequency modulation (PFM), with the converter operating in discontinuous conduction mode (DCM) at variable switching frequency, is applied at low power levels. The dual-mode operation has been proposed earlier for dc/dc converters operating as fixed voltage regulators [11]–[13]. In this paper, this technique is extended to the converter that operates over a wide range of output voltages.

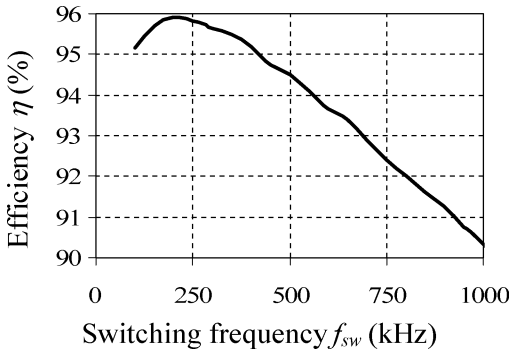

Fig. 2. Experimental efficiency of the dc/dc converter as a function of the switching frequency f_{sw}.

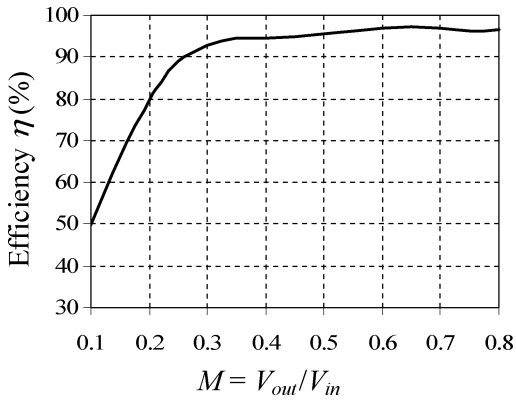

Fig. 3. Experimental efficiency of the dc/dc converter operating in CCM, as a function of the conversion ratio, $M = V_{\rm out}/V_{\rm in}$.

Digital controller implementation for high-frequency dc/dc converter applications has recently received significant attention. In this paper, we extend the digital controller approach [14]–[16] to the dual-mode operation including PFM mode at light loads and operation over the wide range of output voltages. In the system of Fig. 1, in addition to the flexibility of programmable system parameters, including the compensator parameters and the mode transition parameters discussed in Section IV, the digital controller allows implementation of additional RFPA control functions such as predistortion [2] or active ripple cancellation [3].

The paper is organized as follows. Section II describes the CCM and PFM modes of operation and mode switching, based on experimental efficiency results. The field-programmable gate array (FPGA)-based digital controller implementation in the system of Fig. 1 is introduced in Section III. Section IV presents details of the experimental test circuit, as well as the CCM and the PFM controller implementation. Experimental results are presented in Section V. In the complete closed-loop power control system shown in Fig. 1, which consists of the digitally controlled dc/dc converter and the class-E RFPA operating at 10 GHz [4], the experimental results show that the overall system efficiency is significantly improved over the wide range of RFPA output power.

II. Converter Operating Modes for High Efficiency Over a Wide Range of Output Power

The drain supply voltage $V_{\rm out}$ of the RFPA is provided by a synchronous dc/dc buck converter. Since the RFPA is a high-efficiency switched-mode class-E power amplifier, it presents an approximately constant resistive load for the converter [9], [10] ($R_{\rm Load} = 100\ \Omega$ in our experimental system). The RFPA output power varies by changing the converter output voltage $V_{\rm out}$. At high load the converter operates in CCM.

Fig. 2 shows the experimental efficiency of the dc/dc converter operating in CCM as a function of the switching frequency f_{sw} in the range from 100 kHz to 1 MHz. In this experiment, $V_{\rm in} = 5$ V, $V_{\rm out} = 2.5$ V, $L = 30\ \mu$H, $C = 25\ \mu$F. For the experimental prototype operating in CCM, we selected the switching frequency $f_{sw} = 200$ kHz, which results in the best efficiency and meets the ripple (20 mV) and bandwidth (10 kHz) requirements. At this switching frequency, the filter inductance $L = 30\ \mu$H results in zero voltage switching (ZVS) [18], [19], with reduced switching losses.

Fig. 3 shows the experimental efficiency result for the constant-frequency ZVS converter operating in CCM at the switching frequency of $f_{sw} = 200$ kHz, as a function of the dc conversion ratio M.

It can be observed that the converter efficiency is very high for intermediate and high output voltages. At low output voltages, which correspond to the low RFPA output power levels, the CCM converter efficiency drops down dramatically because of the switching losses. To improve the light-load efficiency, the converter can be operated in a pulse frequency modulation (PFM) mode. In the PFM mode, the converter operates in DCM at a switching frequency that depends on the load. For dc/dc converters designed to regulate the output voltage at a constant reference value, such PFM mode has been applied often, such as in [7], [8], [11]–[13].

For a fixed output voltage, the converter in PFM applies a constant charge to the load in each switching cycle. When the load current varies, the frequency of the charge delivery to the load varies in proportion to the load current. In our application, since the RFPA presents an approximately constant resistive load for the converter, the converter output voltage must be dynamically adjusted in a wide range to provide different values of the RFPA output power. Because of the output voltage variation, the constant charge idea in PFM is no longer applicable. Different approaches to achieve PFM operation include operation at constant inductor peak current I_p, constant on time $t_{\rm on}$, or constant off time $t_{\rm off}$ of the high-side switch Q_1. Based on the converter DCM waveforms [20], the PFM switching frequency f_{sw} as a function of the output voltage variation can be easily found as

$$f_{sw} = \frac{2L}{t_{\rm on}^2 R_{\rm Load}} \cdot \frac{M^2}{1-M} \tag{1}$$

$$f_{sw} = \frac{2L}{t_{\rm off}^2 R_{\rm Load}} \cdot (1-M) \tag{2}$$

$$f_{sw} = \frac{2V_{\rm in}}{LI_P^2 R_{\rm Load}} \cdot M^2(1-M) \tag{3}$$

for constant $t_{\rm on}$, constant $t_{\rm off}$, and constant I_p, respectively, where

$$M = \frac{V_{\rm out}}{V_{\rm in}} \tag{4}$$

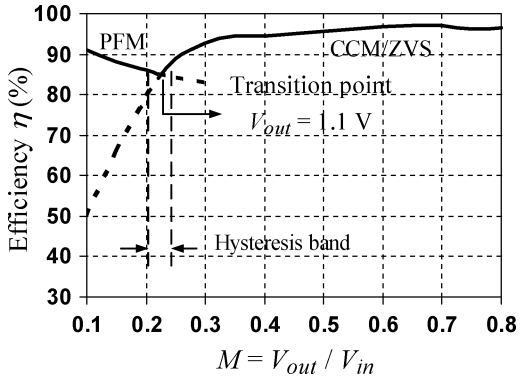

Fig. 4. Measured converter efficiency as a function of the conversion ratio $M = V_{\rm out}/V_{\rm in}$, for two modes of operation: PFM and CCM.

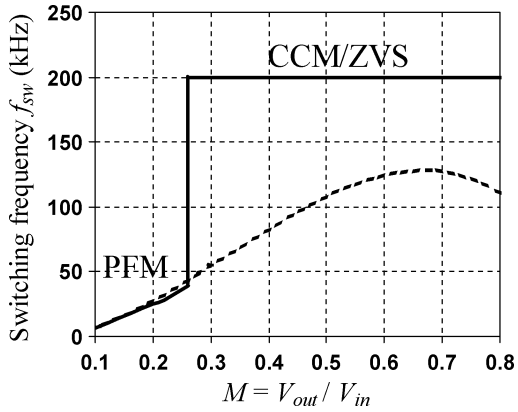

Fig. 5. Measured converter switching frequency (solid line) and the PFM switching frequency found from (3) (dashed line) as functions of the conversion ratio $M = V_{\rm out}/V_{\rm in}$.

is the conversion ratio. For the purpose of maintaining high efficiency over a range of output voltages in PFM, the switching losses and therefore the switching frequency should scale in proportion with the load power, i.e., in proportion with the square of the conversion ratio M. In the constant $t_{\rm off}$ approach, the switching frequency f_{sw} increases with decreasing M, which is undesirable. In the constant $t_{\rm on}$ approach, for low M, (1) shows that the switching frequency is approximately proportional to M^2. However, the inductor peak current in the constant $t_{\rm on}$ approach increases to a high value at low output voltages, which results in increased conduction losses and the output voltage ripple. For the constant inductor peak current control, at low M, we observe from (3) that the PFM switching frequency is approximately proportional to M^2, which is the most favorable behavior. Therefore, the constant I_p control was selected for PFM implementation.

To maintain the highest possible efficiency at all power levels, it is desirable to switch between the CCM and PFM modes depending on which mode of operation results in higher efficiency. Fig. 4 shows the experimental converter efficiency as a function of the conversion ratio M for the two modes of operation. From Fig. 4, we found that the PFM efficiency is greater than the CCM efficiency for $V_{\rm out}$ less than approximately 1.1 V (M less than 0.22, given $V_{\rm in} = 5$ V). Given that the RFPA presents an approximately constant load resistance $R_{\rm Load}$ at the output of the converter, simply monitoring the output voltage $V_{\rm out}$ can be used to switch between the modes. In the practical implementation, which is described in Sections III and IV, a small hysteresis band around the transition point prevents repeated mode switching when the converter operates in the neighborhood of the transition point.

The switching frequency in the experimental converter is shown in Fig. 5 as a function of the conversion ratio M. At low output voltages, the converter operates in PFM and the measured switching frequency closely follows the expression (3). At the transition point, the switching frequency f_{sw} is increased abruptly to 200 kHz, and the converter operates in zero voltage switching CCM at constant frequency.

III. System Implementation

A block diagram of the complete system implementation is shown in Fig. 6. The mode switching and the control in CCM

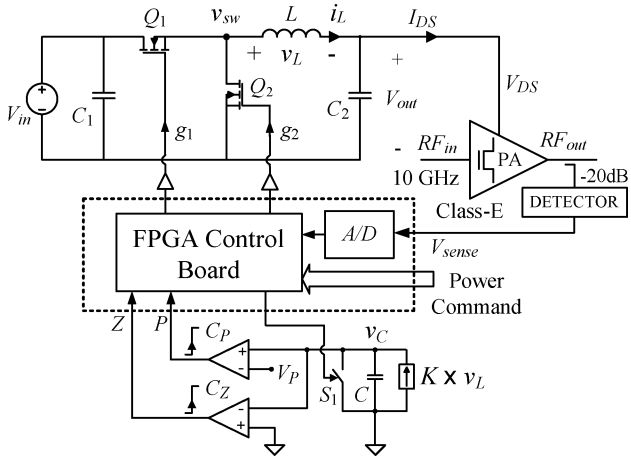

Fig. 6. System block diagram.

and PFM modes are accomplished using an FPGA-based digital controller. The system includes the synchronous buck converter, the RFPA, a current estimator circuit, the digital controller, and an A/D converter. The FPGA control board includes a Xilinx Virtex II (XC2V1000 chip). The X-band class-E RFPA design has been reported in [4]. The signal $V_{\rm sense}$ obtained from a detector at the output of the RFPA is A/D converted and compared with a digital power command. For $V_{\rm out} > 1.1$ V, the digital controller operates in CCM as a constant-frequency voltage-mode pulse-width modulator (PWM) controller. For the power command which corresponds to the output voltage $V_{\rm out} < 1.1$ V, the converter is switched to the PFM mode with approximately constant inductor peak current I_P.

The system in Fig. 6 performs closed-loop RFPA output power control. In steady state, the output voltage of the dc/dc converter is adjusted so that the RFPA output power measured by the detector equals the power command value.

The basic CCM and PFM operation, as well as the mode switching function described in Section II can be realized using traditional analog circuit techniques. The main reasons for the digital controller implementation described in this paper are the following: a) flexibility of programming and testing various system parameters, such as compensator parameters, switching frequency, mode-switching transition point, and

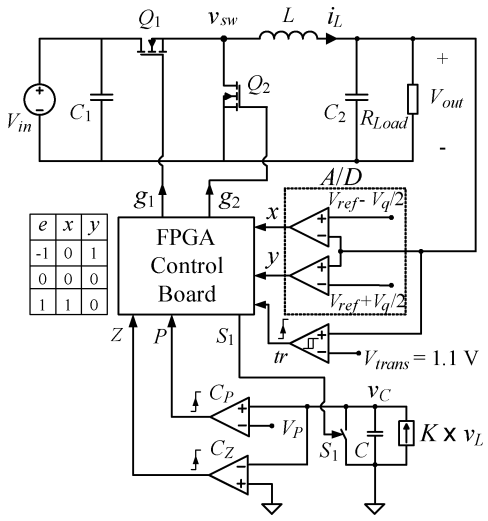

Fig. 7. Experimental test circuit.

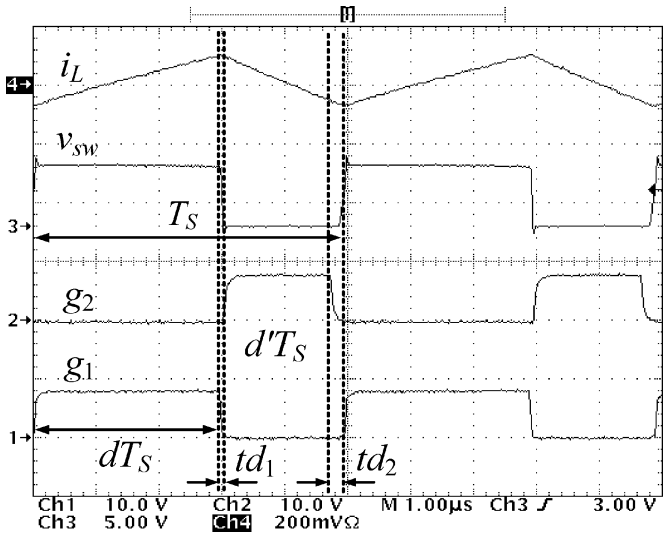

Fig. 8. Measured waveforms in the synchronous buck converter operating in CCM. $V_{\rm in} = 5$ V, $V_{\rm out} = 3$ V, $f_{sw} = 200$ kHz.

switch dead times, b) ability to control the switch timing at the PFM/CCM transition point, to minimize effects of the abrupt mode switching and the abrupt switching frequency change on the output voltage, and c) ability to use the same controller hardware to perform other RFPA control functions, such as linearization of the RFPA output power detector characteristic, predistortion [2] or active ripple cancellation [3]. Furthermore, in a battery-powered electronic system, the digital controller described here would be well suited for low-cost implementation on a digital CMOS baseband controller chip.

IV. Experimental Test Circuit

The experimental circuit used to test the controller and the synchronous buck converter operation is shown in Fig. 7. The RFPA is replaced with a constant resistive load of $R_{\rm Load} = 100\ \Omega$ An external analog voltage source $V_{\rm ref}$ is used instead of the RFPA detector and the power command. The test circuit operates as a dc/dc voltage regulator with the output voltage regulated at $V_{\rm ref}$. Details of the operation in the two modes, the zero-voltage-switching CCM and the PFM, are described in this section.

A. Zero Voltage Switching CCM Operation at Constant Switching Frequency

As discussed in Section II, the synchronous buck converter operates at constant switching frequency in zero-voltage switching CCM for $V_{\rm out} > 1.1$ V. The filter inductor $L = 30\ \mu$H is selected so that the inductor current ripple results in zero-voltage switching of the MOSFET's Q_1 and Q_2 [18], [19]. Fig. 8 shows experimental steady-state waveforms in the dc/dc converter operating in CCM: the inductor current i_L, the switching waveform v_{sw}, and the gate drive signals g_1 and g_2. During the dT_s portion of the switching period T_s, the MOSFET Q_1 is turned on and the inductor current ramps up. When the MOSFET Q_1 is turned off, the inductor current discharges the parasitic capacitance at the v_{sw} node. After a short delay td_1 the switching voltage v_{sw} drops to zero, and the synchronous rectifier Q_2 is turned on at zero voltage. During the $d'T_s$ portion of the switching period, the MOSFET Q_2 is on and the inductor current ramps down. At the end of the $d'T_s$ interval, the inductor current has reversed polarity. As a result, when Q_2 is turned off, the inductor current charges the parasitic capacitance at the v_{sw} node, which allows zero-voltage turn-on of the MOSFET Q_2 after a short delay td_2. The gate drive waveforms g_1 and g_2, which include the delays td_1 and td_2 necessary for ZVS operation, are generated by the digital controller.

The output capacitor filter is chosen such that the output voltage ripple does not exceed 20 mV. With the given values of L, $V_{\rm in}$, $V_{\rm out}$, f_{sw} and $C = 25\ \mu$F, the maximum peak-peak output voltage ripple is less than 6 mV.

The digital CCM controller implemented on the FPGA is a voltage-mode PID controller that follows the techniques described in [15], [16]. It consists of a very simple two-comparator flash A/D converter, a look-up table based compensator, and a 9-b constant-frequency (200 kHz) digital pulse-width modulator (DPWM).

The digital error signal e corresponds to the digital signals x and y at the outputs of the two A/D comparators as shown in Fig. 7. For output voltages between $V_{\rm ref} - V_q/2$ and $V_{\rm ref} + V_q/2$ the comparator outputs are $x = 0$ and $y = 0$, which corresponds to the zero error $e = 0$. In the experimental test circuit, the zero-error bin is $V_q = 40$ mV. The voltage values outside the zero-error bin result in the digital error of $+1$ or -1.

The digital compensator computes the duty-cycle command based on the digital error signal $e[n]$ in the current switching cycle, and the previous two switching cycles, $e[n-1]$, $e[n-2]$. The discrete-time compensator is designed starting from a continuous-time design using the pole-zero mapping approach [21].

The averaged model of the buck converter in constant-frequency CCM [20] gives the following control to output transfer function:

$$G_{vd}(s) = \frac{V_{\rm in}}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2}. \tag{5}$$

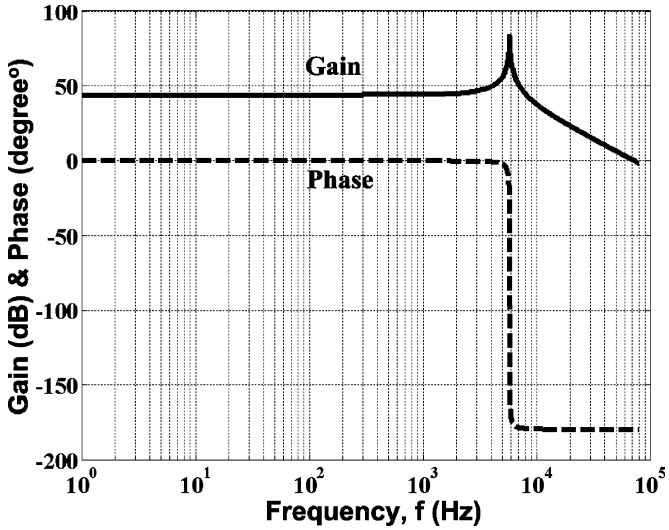

Fig. 9. Bode plots of the control to output transfer function of the buck converter operating in CCM. $L = 30\ \mu$H, $C = 25\ \mu$F.

For the buck converter with $L = 30\ \mu$H and $C = 25\ \mu$F, $R = 100\ \Omega$, the magnitude and phase responses of $G_{vd}(s)$ are shown in Fig. 9.

A continuous-time PID compensator is designed to give an appropriate loop gain with a crossover frequency of $f_c = 10$ kHz, phase margin $\phi_m > 60^\circ$, and very high dc gain

$$G_{\rm comp}(s) = K_{\rm comp}\frac{1+\frac{s}{Q_{\rm comp}\omega_z}+\left(\frac{s}{\omega_z}\right)^2}{s}. \tag{6}$$

In the experimental prototype, we have: $f_z = 4.5$ kHz and $Q_{\rm comp} = 2$. To implement the control law in the FPGA, the discrete form of above PID compensator is obtained using the pole-zero mapping method [21]

$$G_{\rm comp}(z) = \frac{a+bz^{-1}+cz^{-2}}{1-z^{-1}}. \tag{7}$$

From (7), the discrete-time equivalent of the PID compensator has the following form:

$$d[n] = d[n-1] + ae[n] + be[n-1] + ce[n-2] \tag{8}$$

where $e[n]$, $e[n-1]$, $e[n-2]$ are the digital error signals, $d[n-1]$ is the digital duty-cycle command stored from the previous cycle, and $d[n]$ is the current duty cycle command. The compensator coefficients a, b and c are found by the pole-zero mapping method as

$$b = -a\cdot 2r\cdot\cos\left(2\pi\frac{f_z}{f_{sw}}\sqrt{1-\frac{1}{(2Q_{\rm comp})^2}}\right) \tag{9}$$

$$c = a\cdot r^2 \tag{10}$$

$$r = \exp\left(-\frac{\pi f_z}{Q_{\rm comp}f_{sw}}\right). \tag{11}$$

The value of the coefficient a is determined such that the magnitude response of the discrete-time implementation matches the magnitude response of the continuous-time compensator (6) at the desired crossover frequency f_c.

Given the switching frequency of $f_{sw} = 200$ kHz, and the parameters $f_z = 4.5$ kHz, $f_o = 5.8$ kHz, $Q_{\rm comp} = 2$ and the desired values of the crossover frequency $f_c = 10$ kHz, and the phase margin $\phi_m > 60^\circ$, the discrete-time compensator coefficients are found as

$$\begin{aligned} a &= 0.05,\\ b &= -0.09543,\\ c &= 0.04651. \end{aligned} \tag{12}$$

These values correspond to the assumption that the digital duty-cycle command d[n] is between 0 and 1, in which case we have that the DPWM gain equals 1. Based on the coefficient values (12), a look-up table is used in the FPGA to store the duty-cycle correction

$$d_c = ae[n] + be[n-1] + ce[n-2] \tag{13}$$

for all possible values $(-1, 0, 1)$ of the three error signals, $e[n]$, $e[n-1]$, $e[n-2]$. In each switching period, only one addition is required to complete the PID compensator calculation (8). Table I shows the complete set of correction values for all possible error signals. As shown in Fig. 7, the digital error signal e is obtained from the A/D comparator outputs x and y.

Fig. 10 shows the complete system loop gain, demonstrating the crossover frequency of 12 kHz and the phase margin $\phi_m = 67^\circ$. To obtain these plots, the equivalent A/D gain of $1/V_q$ is taking into account, neglecting quantization effects. Since the two-comparator A/D converter has only three error bins, it should be noted that the loop gain result given in Fig. 10 is relevant only when the output voltage is located in the vicinity of the

TABLE I
DUTY COMMAND CORRECTION VALUES FOR ALL POSSIBLE VALUES OF ERROR SIGNALS e

Index	e [n]	e [n-1]	e [n-2]	d_c
1	-1	-1	-1	-0.00108
2	-1	-1	0	0.04543
3	-1	-1	1	0.09194
4	-1	0	-1	-0.09651
5	-1	0	0	-0.05
6	-1	0	1	-0.00349
7	-1	1	-1	-0.19194
8	-1	1	0	-0.14543
9	-1	1	1	-0.09892
10	0	-1	-1	0.04892
11	0	-1	0	0.09543
12	0	-1	1	0.14194
13	0	0	-1	-0.04651
14	0	0	0	0
15	0	0	1	0.04651
16	0	1	-1	-0.14194
17	0	1	0	-0.09543
18	0	1	1	-0.04892
19	1	-1	-1	0.09892
20	1	-1	0	0.14543
21	1	-1	1	0.19194
22	1	0	-1	0.00349
23	1	0	0	0.05
24	1	0	1	0.09651
25	1	1	-1	-0.09194
26	1	1	0	-0.04543
27	1	1	1	0.00108

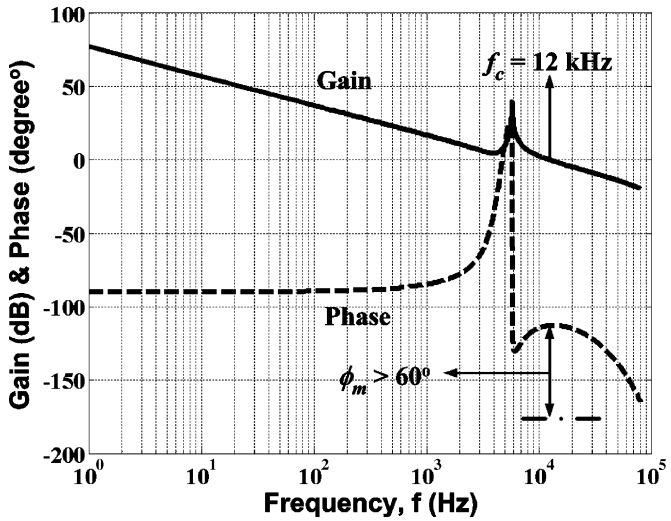

Fig. 10. Magnitude and phase responses of the loop gain for the digitally controlled buck converter operating in CCM.

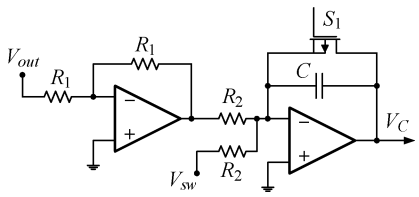

Fig. 11. Details of the current estimator circuit.

A/D zero error bin, i.e., when the output voltage is in or close to regulation. If the output voltage is outside of the zero error bin for more than three switching cycles, the look-up table compensator behaves as a simple integrator resulting in relatively slow but stable closed-loop response.

B. PFM Operation

The synchronous buck converter operates in PFM mode for $V_{\rm out} < 1.1$ V. The PFM mode is a DCM where the main switch Q_1 is turned off when the inductor current reaches a constant peak value I_p. The synchronous rectifier Q_2 must be turned off when the inductor current reaches zero. Instead of sensing the inductor current, which may result in additional losses and sensitivity to noise, a simple analog current estimator shown in Fig. 7 is designed to obtain a voltage waveform proportional to the inductor current, as in [12] and [17]. The circuit consists of a dependent current source proportional to the inductor voltage, and an integrating capacitor C. Fig. 11 shows details of the inductor current estimator circuit.

The relation between the integrating capacitor peak voltage, V_P, and inductor peak current I_P is:

$$I_P = \alpha V_P \tag{14}$$

where

$$\alpha = \frac{R_2 C}{L}. \tag{15}$$

Fig. 12 shows experimental waveforms in the synchronous buck converter operating in PFM: the inductor current i_L, the current estimator capacitor voltage v_C, the switching waveform

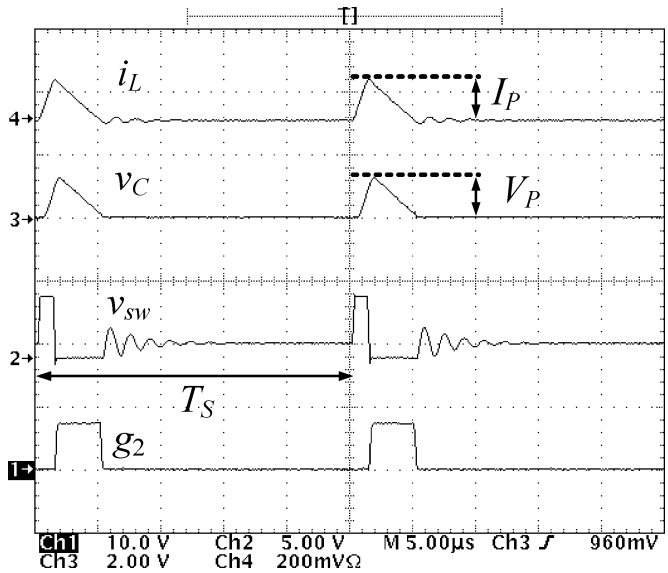

Fig. 12. Measured waveforms in the synchronous buck converter operating in PFM. $I_P = 120$ mA, $V_P = 1.2$ V, $V_{\rm in} = 5$ V, $V_{\rm out} = 1$ V, $f_{sw} = 40$ kHz.

v_{sw}, and the gate drive signal g_2. At the beginning of each switching period, MOSFET Q_1 is turned on and the switch S_1 is turned off. The inductor current i_L and the integrating capacitor voltage v_C ramp up. When the capacitor voltage v_C reaches the programmed peak value V_P, the logic signal P changes its level from zero to one, the MOSFET Q_1 is turned off and the synchronous rectifier Q_2 is turned on. As a result, the inductor current i_L and the capacitor voltage v_C ramp down. When the capacitor voltage v_C reaches zero, the logic signal Z changes its level from zero to one, and the digital controller turns off the synchronous rectifier Q_2 and turns on the switch S_1 to reset the integrating capacitor to zero. The cycle is repeated when the output voltage $V_{\rm out}$ drops below the reference value $V_{\rm ref}$.

The digital controller for PFM is implemented as a simple state machine on the FPGA.

In the experiment, the maximum inductor peak current is set to $I_p = 120$ mA, which results in the output voltage ripple of less than 20 mV in PFM.

V. Experimental Results

A. Controller and Converter Waveforms

Fig. 13 shows the output voltage $V_{\rm out}$, the reference $V_{\rm ref}$ and the transition between the CCM and PFM modes of operation. The reference voltage changes between 0.5 V and 5 V. At low output voltages the digitally-controlled converter operates in variable-frequency PFM mode. At higher output voltages, the digitally-controlled converter operates in constant-frequency zero-voltage-switching CCM. The hysteresis band around the CCM/PFM transition point (1.1 V) can be observed. It can also be observed that the output voltage tracks the reference precisely in both modes of operation. There is no significant disturbance in the output voltage at the mode switching point.

Fig. 14 shows a detail of the converter waveforms around the mode switching point: the switching voltage v_{sw}, the output voltage $V_{\rm out}$, the inductor current i_L, and the mode logic signal (high= CCM, low= PFM). It is interesting to note how the

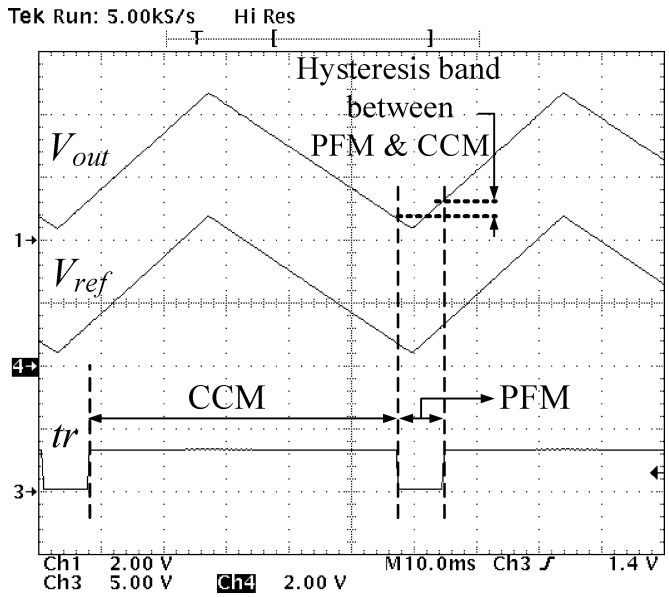

Fig. 13. The output voltage $V_{\rm out}$, the reference voltage $V_{\rm ref}$, and the mode logic signal (high = CCM, low = PFM) in the experimental digitally controlled syncronoud buck converter.

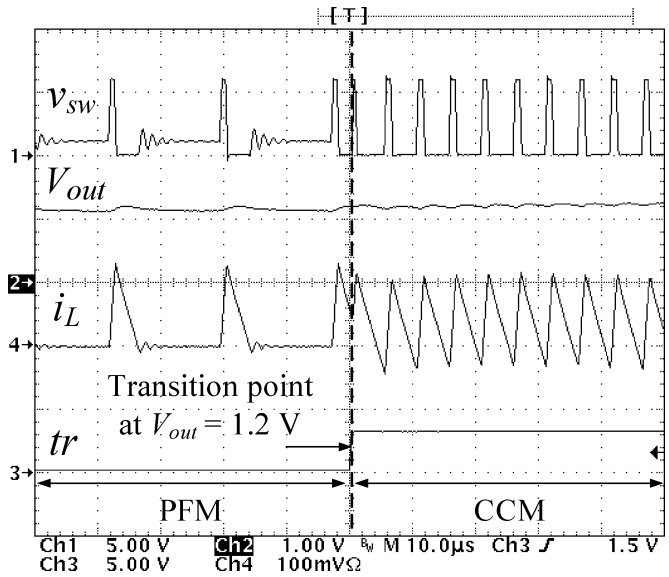

Fig. 14. Switching voltage v_{sw}, the output voltage $V_{\rm out}$, the inductor current i_L, and the mode logic signal (high= CCM, low=PFM) in the experimental digitally controlled buck converter. The mode switching occurs at $V_{\rm out}$ = 1.2 V. The initial value of the duty ratio in the first CCM cycle after the transition from PFM is programmed to minimize the disturbance in the output voltage.

inductor current transitions from discontinuous mode (in PFM) to continuous mode operation. At the point of switching from PFM to CCM, the initial value of the duty cycle in the first CCM period is programmed in the digital controller to a value that attempts to minimize the inductor current transient.

Fig. 15 shows the same waveforms as in Fig. 14, except that the initial value of the duty cycle in the first CCM period is arbitrarily set to a value away from the value that minimizes the PFM/CCM transient. Transient waveforms of the output voltage and the inductor current indicate that in this case the converter operates out of regulation for a number of cycles. The smooth

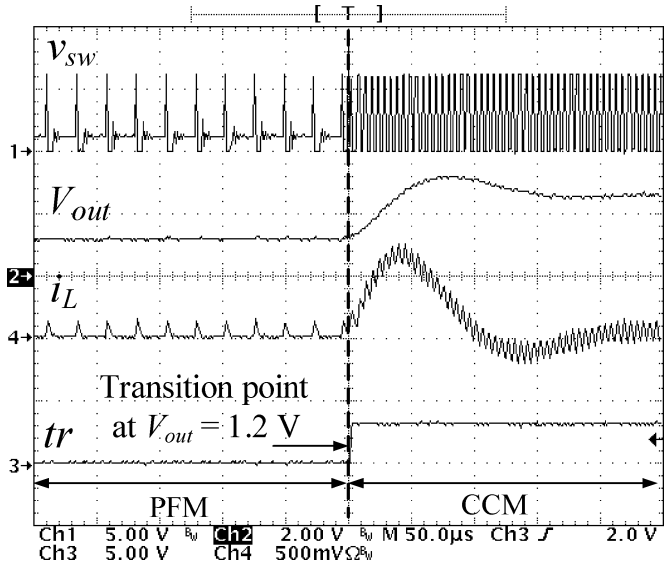

Fig. 15. Switching voltage v_{sw}, the output voltage $V_{\rm out}$, the inductor current i_L, and the mode logic signal (high=CCM, low=PFM) in the experimental digitally controlled buck converter. The mode switching occurs at $V_{\rm out}$ = 1.2 V.

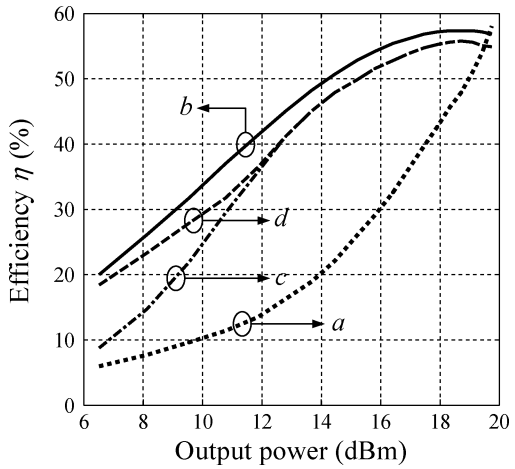

Fig. 16. Experimental system efficiency results: (a) RFPA is supplied from a constant voltage V_{DS}, (b) the supply voltage of the RFPA, V_{DS} is varried dynamically from an ideal 100% efficient power supply, (c) the RFPA is supplied by the dc/dc converter operating in CCM over the entire range of output power, and (d) the RFPA is supplied by the dual-mode PFM/CCM dc/dc converter.

transition in Fig. 14 illustrates an advantage of the digital controller where the optimum value of the duty cycle can be easily programmed.

B. System Efficiency

The digitally controlled dc/dc converter has been used to provide the supply voltage for the class-E RF power amplifier operating at 10 GHz [4] as shown in the system block diagram of Fig. 6. Fig. 16 shows the measured efficiency of the entire system as a function of the RF output power in dBm. This efficiency is compared with the efficiency of the RFPA operating with a constant supply voltage. The efficiency results include the total power supplied to the drain and to the input port of the RFPA.

The efficiency curve "*b*" is obtained assuming that the RFPA is supplied from an ideal 100% efficient variable-voltage source.

The efficiency curve "c" is obtained when the RFPA is supplied with the dc/dc converter operating in CCM only and "d" when the converter is operated in the PFM or CCM, as described in Section II. The results show a significant improvement in efficiency at low power levels. The small difference between the efficiency curves "b" and "d" shows that the highly efficient dc/dc converter introduces only a small penalty in overall system efficiency compared to the ideal case.

VI. Conclusion

This paper describes design and implementation of a digitally controlled synchronous buck dc/dc converter that provides a dynamically adjustable supply voltage for an RFPA. In this application, the dc/dc converter has to operate over a wide range of output voltages, and over a correspondingly wide range of output power. A combination of constant-frequency zero-voltage-switching CCM, and variable-frequency DCM (pulse frequency modulation, or PFM) is employed to achieve high converter efficiency over the wide range of output power levels. Since the RFPA presents an approximately constant resistance at the output of the dc/dc converter, the switching between the modes is accomplished simply by monitoring the output voltage. The mode transition point is selected to maximize the converter efficiency.

The FPGA-based digital controller allows programmability of the mode transition point, compensator, and other controller parameters, as well as implementation of other RFPA control functions. In constant-frequency CCM, the switching frequency is 200 kHz and the controller includes a simple two-comparator A/D converter, a table-based discrete-time PID compensator and a 9-b digital PWM. In PFM, the peak inductor current is approximately constant, and the switching frequency is adjusted to maintain the output voltage control. A simple analog current estimator is used to accomplish switching of the main power switch and the synchronous rectifier without the need to sense the inductor current. The PFM digital controller is implemented as a simple state machine. Experimental waveforms show that the switching between the modes of operation is automatic and smooth, without significant disturbances observed in the output voltage.

In the complete experimental system, which consists of the digitally controlled dc/dc converter and a class-E RFPA operating at 10 GHz, experimental results show that the overall system efficiency is significantly improved over a wide range of RFPA output power levels.

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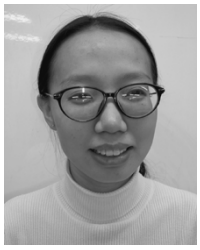

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