

A 2 Gb/s $\Delta\Sigma$ Directly Driven Wireless Link

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Abstract—One-bit $\Delta\Sigma$ modulation in a wireless transmitter is studied as a potential candidate for multifunction broadband transmit front ends. Characterizing a single $\Delta\Sigma$ modulated transmit element is the first step towards a transmit array for radar/communication applications. A wireless link directly driven by a 2 Gb/s $\Delta\Sigma$ bit sequence is analyzed through simulation and measurement. Effects of clock jitter, asymmetrical rise/fall edges and asymmetrical rise/fall times of the digital signal are studied. A Xilinx Virtex II-Pro FPGA is used to generate the $\Delta\Sigma$ bit sequences. The transmit and receive antennas simultaneously perform bandpass filtering of the noise in the $\Delta\Sigma$ spectrum.

Index Terms—Delta-Sigma Modulation, Multifunction Array, Wireless Transmitter

I. INTRODUCTION

As a result of the increased use of the RF spectrum for communication and sensing, the density of antennas on a variety of platforms has been continuously increasing. For example, nuclear aircraft carriers (CVNs) have as much as 150 antennas on board, resulting in interference, increase of radar cross-section and emissivity, signal masking and obstruction, and increasing maintenance [1]. A possible solution for this collocated antenna problem is a multifunctional and/or reconfigurable transmit and receive system. Multifunctional antenna arrays that can perform radar, electronic warfare, information warfare and communication functions simultaneously are desirable.

A number of receiving multifunctional arrays have been discussed, e.g. the Advanced Multifunction RF Concept (AMRF-C) has shown the ability to form multiple simultaneous beams in receive mode [2][3]. In transmit mode, however, the combined need for high power, linearity and bandwidth make the problem more challenging. $\Delta\Sigma$ modulation provides a promising approach because it can in theory achieve high linearity by spectral shaping of quantization noise from a low-resolution (2-level) quantizer [4][5]. The coded output waveform is thought to be less sensitive to nonlinearities which allows use of nonlinear amplifiers to achieve high power, high efficiency and high linearity of the transmitted signals. This approach also follows the trend to move the digital/analog boundary closer to the antenna element.

Most of the research in this field to date are simulations, due to the difficult requirements on the electronic hardware in terms of digital clock rates [6]-[9]. This paper presents simulations and measurements for a directly-transmitted RF frequency $\Delta\Sigma$ modulated signal. A high performance commercial Field Programmable Gate Array (FPGA) is used to generate

2 Gb/s $\Delta\Sigma$ bit sequences. Retiming circuitry is implemented to reduce jitter, and a variety of hardware effects on the SNR are studied. Since many potential applications, such as radar and arbitrary waveform generation, require pulsed or repeated waveforms, the effect of finite length $\Delta\Sigma$ sequences on output signal spectra are examined here.

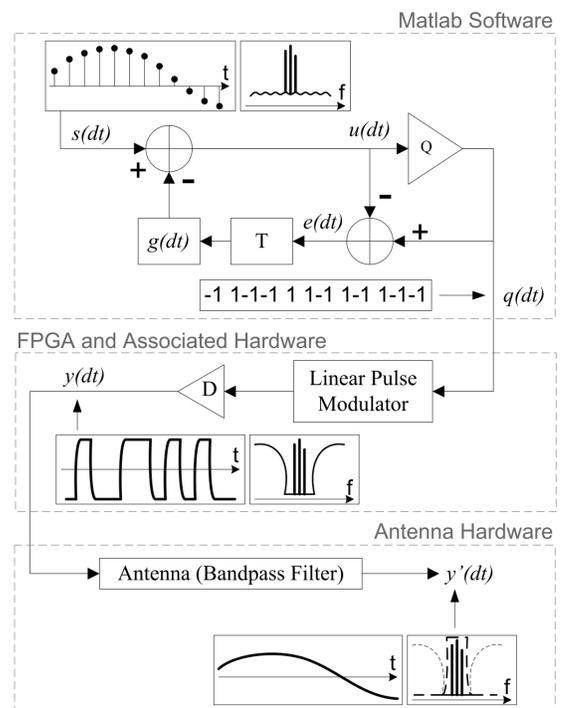


Fig. 1. Digitized three-tone signal $s(dt)$ is $\Delta\Sigma$ encoded in software resulting in a one-bit digital signal $q(dt)$. The digital signal is converted to a higher power analog signal $y(t)$ through a driver circuit. A sketch of the time domain signal and noise shaped spectrum are shown in the inset. The antenna that follows is a bandpass filter which filters the noise and radiates the signal $y'(t)$.

II. IDEAL $\Delta\Sigma$ DAC TRANSCIEVER SINGLE CHANNEL

The single channel system, which is the focus of this paper, is shown in Fig. 1. The data presented here is obtained without the high power driver (D). The quantization noise due to one bit quantization is shaped in the frequency domain to be out of band of the signal that is radiated by the antenna. The *noise-shaping function* h and its Fourier transform H are defined

as

$$h(dt) = \delta(dt) - g(dt - T), \quad H(f) = 1 - G(f)e^{-j2\pi fT} \quad (1)$$

The output signal of the $\Delta\Sigma$ modulator, q , and its *power spectral density* (PSD) R_q are

$$q(dt) = s(dt) + (h * e)(dt), \quad R_q(f) = |S(f)|^2 + \sigma^2 |H(f)|^2 \quad (2)$$

where the quantization noise is assumed to be white noise with power spectral density σ^2 . If a non-return to zero (NRZ) digital waveform is used in the linear pulse modulator, and the output bit sequence is limited to a certain length N , the signal y and its PSD R_y can be expressed as

$$y(t) = \frac{1}{2}(q(dt) + 1)w(dt)f(t) \quad (3)$$

$$R_y(f) = \frac{1}{4\|w\|_2^2} |W(f) * S(f)|^2 + \frac{\sigma^2}{4\|w\|_2^2} |W(f)|^2 * |H(f)|^2 + \frac{1}{4\|w\|_2^2} |W(f)|^2 \quad (4)$$

where $q(dt)$ is a binary bit sequence with levels $\{-1, 1\}$, $w(t)$ is a window function with size N , and $f(t)$ is a constant signal in time domain with amplitude 1. The theoretical spectrum $R_y(f)$ is shown in Fig. 2. The band of interest is centered at 500 MHz, which is one quarter of the digital clock rate.

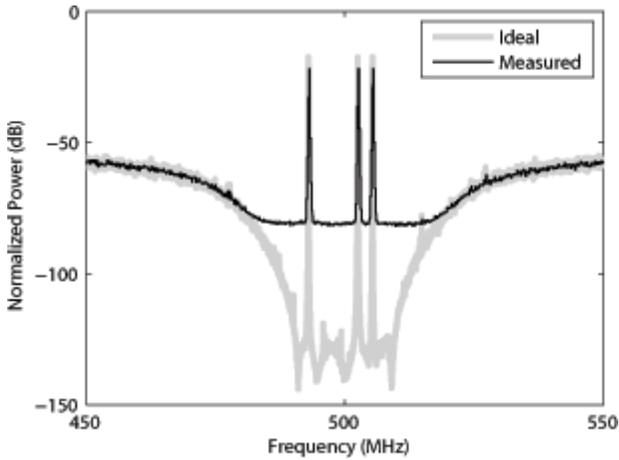


Fig. 2. Ideal $\Delta\Sigma$ spectrum overlaid with our measured spectrum. No realistic hardware can produce the ideal spectrum.

III. IMPLEMENTATION AND RESULTS

The block diagram of the hardware implementation is shown in Fig. 3. The development board has a Virtex-II Pro XC2VP30 hybrid chip which contains both FPGA fabric as well as dual Power PC processors. The chip has RocketIO™ differential serial transceivers capable of a 3.125 Gb/s transmit rate, as well as DDR memory to support large throughput requirements. An external differential clock input allows us to connect an extremely stable clock source, and thereby allows for an arbitrary transmit rate (up to the maximum capability of the hardware). For these experiments, the external clock was set

to 2 GHz to create the 2 Gb/s bit transmit rate. The external clock is configured as the input to the RocketIO™ transceiver, but since the transceiver includes a 20-bit parallel to serial converter (implemented with an on-chip 20x clock multiplier), we set our clock source to the desired switching rate and divide it by 20 with frequency dividers before connecting it to the input of the XUPV2P development board.

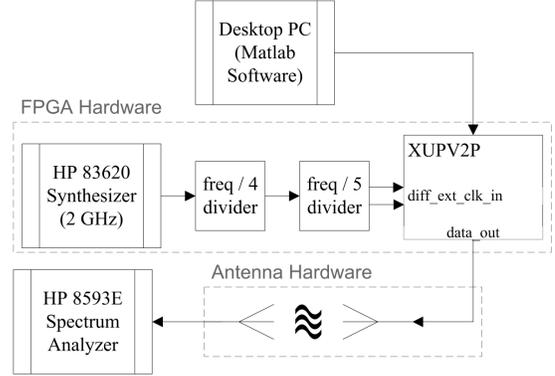


Fig. 3. $\Delta\Sigma$ single channel hardware block diagram. The PC generates the $\Delta\Sigma$ bit sequence. The FPGA hardware generates the $\Delta\Sigma$ waveform. Antenna hardware is the bandpass filter for the signal.

Software running on one of the Power PC cores communicates on a simple RS-232 serial interface to a desktop PC for control and data download. After the user downloads a bit sequence to memory, a looping process is enabled that continually reads data from memory and sends it to the transceiver without interruption. In this way, a pure $\Delta\Sigma$ bit sequence is transmitted continuously. For our measurements, sequence length is limited to 983040 (60/64 of 1 MB) [12].

The output of the FPGA is connected to the transmit half of a wireless link, from which the received signal is captured and displayed by a spectrum analyzer. Fig. 4 shows the spectra of the signals both before and after the wireless link. The transmit and receive antennas are quarter-wave monopoles above one-

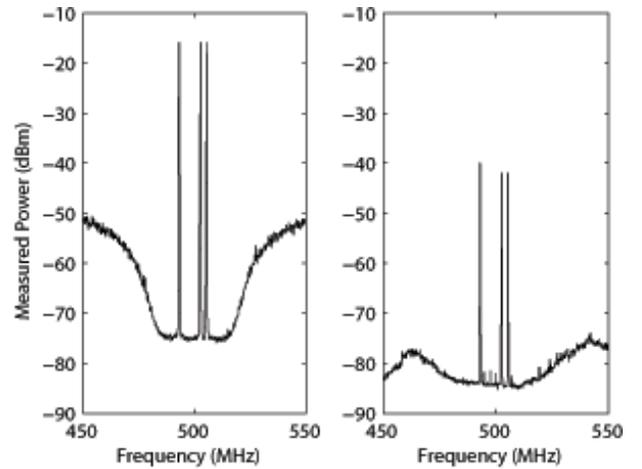


Fig. 4. Measured $\Delta\Sigma$ spectrum before (left) and after (right) the antennas.

wavelength square ground planes. These test antennas have sufficient bandwidth for the sample signal. The wireless link is a bandpass filter, therefore the shaped quantization noise power is filtered before it is radiated. A small amount of the characteristic $\Delta\Sigma$ shape is still discernible in the received spectrum because the antenna does not perform as an ideal filter. Based on the Friis transmission equation, we expect the received power to be at least 22dB lower than the transmitted power, assuming perfect impedance matching, polarization matching, and coplanar monopoles. It can be seen in Fig. 4 that the received power level is about 25dB below the transmitted power, as expected.

IV. INFLUENCE OF HARDWARE

The $\Delta\Sigma$ spectrum is very sensitive to the variance of the waveform generated at the output of the linear pulse modulator. Different nonidealities introduced by the hardware can corrupt the ideal spectrum depending on their relative amplitude level to the expected in-band SNR. Asymmetry of the waveform and random jitter issues are what we mainly focus on in the analysis of influence from hardware because they are the most common problems that degrade the $\Delta\Sigma$ spectrum [10]. All the simulations are done based on the switching characteristics of the RocketIO™ transmitter block on the XUPV2P development board [13].

A. Waveform Asymmetry

Waveform asymmetry of $\Delta\Sigma$ sequences can be interpreted as different rise and fall edge shapes or times. Their effects are simulated in Matlab by using a 10,000 bit three-tone $\Delta\Sigma$ sequence [12]. Fig. 5 shows that the noise shaping spectrum degradation caused by waveform asymmetry is determined by the amplitude of the signal that is the difference of the ideal waveform and the generated waveform, correlated with the ideal waveform. The difference signal for the asymmetric time case can be decomposed into a symmetrical tri-level $\Delta\Sigma$ signal and the remainder, which we call the sub-difference signal as in Fig. 5(c). It is this sub-difference signal that causes the ideal noise notch to be obscured, as shown on the right side of Fig. 5(d).

B. Random Jitter

Random jitter (RJ) is the jitter introduced by the accumulation of random processes inside the system. In our simulation, we analyze the effect of RJ by assuming that it is sufficiently small so as to not cause a bit error in the sequence. From the results shown in Fig. 6, it can be seen that the random jitter effect is similar to the effect of waveform asymmetry in that it also decreases the SNR inside the notch and is determined by the difference signal. However, the RJ shows a much stronger distortion of the spectrum simply because the difference pulse sequence has a much larger amplitude.

From the above results, it can be seen that the influence of the hardware can be quantified based on the difference signal

amplitude and its correlation to the $\Delta\Sigma$ sequence. Random jitter shows a stronger effect on the spectrum degradation. In order to reduce its effect, a cleaner clock source has to be used in signal generation, and retiming circuitry can be added to the output of the linear pulse modulator to decrease the jitter it introduces. To reduce the effect of waveform asymmetry, either a balanced differential configuration system or a different pulse waveform, like RZ pulses, can be used [11]. However, the disadvantages of them are a higher requirement on the circuit symmetry and clock frequency, respectively.

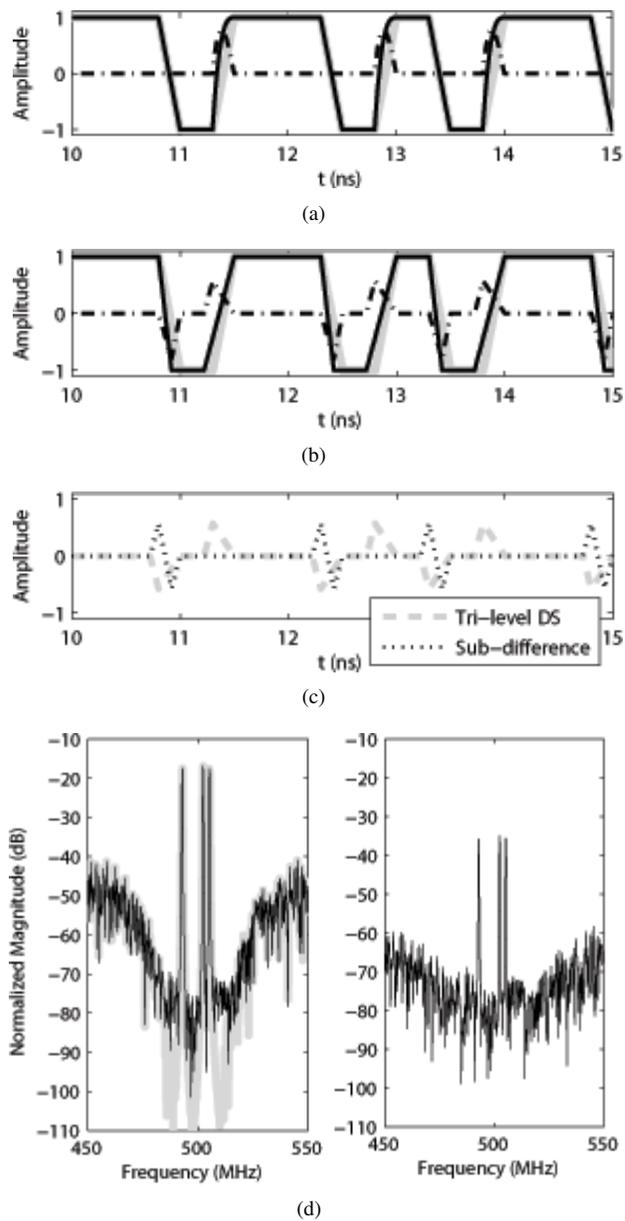


Fig. 5. Simulation results of asymmetric shape (a), asymmetric time (b), components of asymmetric time (c) spectrum of symmetric and asymmetric time (d left), and spectrum of sub-difference signal (d right) waveforms. The thick gray lines are for the ideal case, the thin black lines for the asymmetric case, and the dashed lines represent a signal difference (Parameters chosen based on [13]).

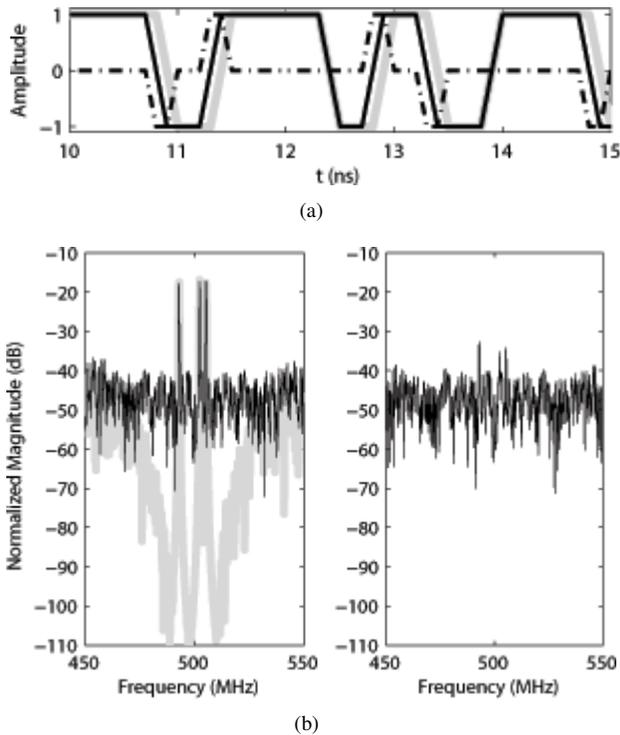


Fig. 6. Simulated random jitter waveform (a), corresponding spectrum (b left), and difference signal spectrum (b right). Legend as in Fig. 5 (Parameters chosen based on [13]).

V. DISCUSSION

As shown in Fig. 6, clock jitter is the major contributor to SNR degradation. Jitter can be related to the phase noise of the clock (oscillator) [14]. The FPGA clock was measured to have a poor phase noise of -65 dBc/Hz at 10 kHz offset, which corresponds to the roughly 50 dB increase in noise floor (Fig. 6). The top plot in Fig. 7 shows the measured eye diagram for this case. When an HP 83620 synthesizer is connected to the external clock input of the FPGA, the eye diagram improves (center plot in Fig. 7). This would correspond to over 20dB improvement in noise floor. To further reduce the effect of jitter, a re-timing circuit is added at the output of the FPGA. The circuit consists of a high-speed D flip-flop (ONsemi MC100EP52) and the resulting eye diagram is shown in Fig. 7 for comparison. The D flip-flop is designed to operate into a broadband 50- Ω load, and thus needs to be matched to operate with the antenna load.

In summary, we have demonstrated a 2 Gb/s directly digitally driven wireless link. Current work is focused on adding a driver for increased transmit power, as well as development of a 12-element digital transmit antenna array with differentially-driven antenna elements.

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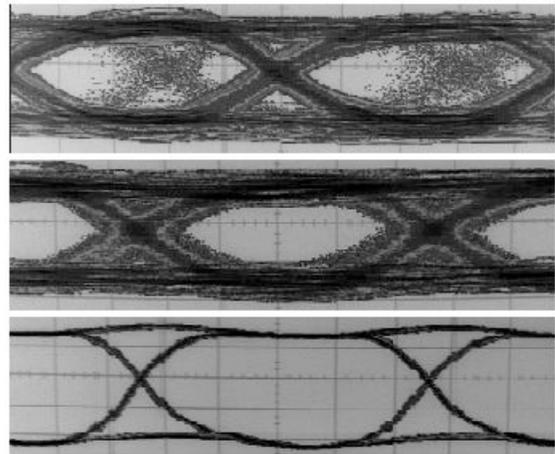


Fig. 7. Measured eye diagrams for on-board clock (top), external clock (center), and external clock with retiming circuit (bottom). Scale is 200 mV/div, 100 ps/div.

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