Electromagnetic Modeling of Wafer-Level Silicon Electro-Optical Packages for 10 & 40 Gb/s Communications

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***Abstract*—This paper presents the electromagnetic (EM) 3-D modeling, hardware measurement, and optimization of hybrid packaged electro-optical transmitters. The initial application is targeted for 10 Gb/s Ethernet and SONET fiber optic communication links. The hybrid package includes a micromachined silicon optical bench, a InP laser and monitor photodiode, a hermetically-sealed lid, integrated impedance-matching resistor, and a flexible RF substrate with additional matching circuits designed to connect to standard driver and control electronics. The measured return loss is better than 10 dB past 10 GHz for two current prototype topologies and simulations show a good match to 40 GHz in a new broadband design.**

I. Introduction

The silicon optical bench (SiOB) is an attractive solution for the fabrication of high-performance telecommunications modules [1]. The ability to batch process the optical subassembly (OSA) through wafer-level processes eliminates much of the costly, serial labor required to produce traditional high-performance optoelectronic modules [2]. In addition, product reliability, assembly automation and yield are improved because of the precise feature definition achievable using photolithography. Historically, SiOB has been used as a component that is inserted into metal or ceramic hermetic packages. Initial work by Rohm and Haas Electronic Materials (RHEM) to convert the SiOB into a hermetic package by sealing a micromachined lid to the SiOB, along with initial environmental testing results, were previously reported in [3] and is being commercialized under the Si-Pak trademark. This approach allows hundreds to thousands of laser transmitters and receivers, complete with micro-optics and thin film electronics, to be fabricated, assembled, sealed, and tested at wafer or grid levels. This paper focuses on the electromagnetic 3-D modeling, simulation, measurement, and layout optimization for next-generation hermetic silicon packages. The initial goal of 10 Gb/s Ethernet and SONET directly modulated laser (DML) transmitters is successfully demonstrated with simulations in good agreement. Design optimizations extended to 25 Gb/s or 40 Gb/s applications are also presented.

Impedance matching in high-bandwidth optoelectronic systems is important for reduced power consumption of the system and to maintain the signal integrity of the waveforms and transmitted optical signal [4]. The exact requirements are dependent on the targeted application (i.e. transmitter optical eye mask margin); however, a return loss better than 10 dB over the frequency range is typically considered adequate.

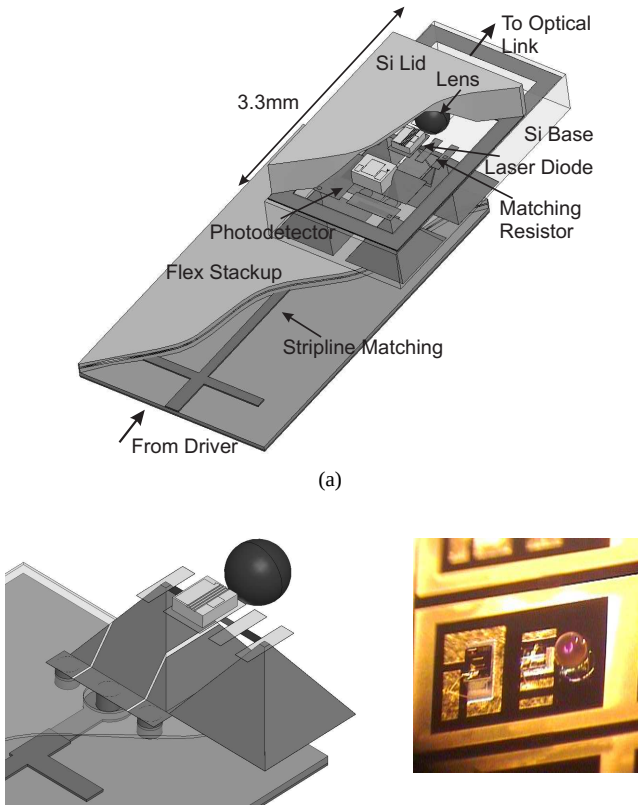


Fig. 1. A sketch of the silicon package (a) with the pertinent features identified. For clarity, the lid and flex stack-up have been sliced open. (b) Detail of RF vias connecting from flex to SiOB, with patterning on one of the pyramidal vias. The photograph (c) shows a fully populated SiOB without a lid before wafer dicing. The spherical lens is 400 μm in diameter.

In this paper, the electromagnetic modeling developed for

10-Gb/s telecommunications transmit modules is presented. Fig. 1 shows the major design components of interest for the electromagnetic performance. The silicon base is processed on both the front and back sides. The silicon lid is processed on a separate wafer. The two wafers are bonded and diced, allowing for a highly parallelized and thus low-cost process. This gives module densities of 10 to 15 devices per cm^2 on the wafers prior to dicing. After dicing, the discrete silicon package is attached to a multi-layer flexible substrate (flex), providing an attachment to the laser driver IC. The full length of the flex is on the order of 2 cm. The silicon package, after being solder attached to the flex, would be incorporated into a mechanical package (not shown) and aligned to either a fiber or a fiber receptacle to achieve a transmitter optical subassembly (TOSA) for insertion into a transceiver.

The electro-optical design presented here utilizes a base silicon wafer which is locally thinned from one side for each die. The thinned regions are then further processed to create a series of microvias which can be provided on a 200um or less pitch. These vias are hermetically sealed with gold plugs. The wafer top side contains thin film circuits including a matching resistor, solder bond pads, and a precision micromachined region to contain a 400-μm lens. The periphery of each chip contains a bond ring for solder sealing a cavitated silicon lid. A wafer or grid of these bases are populated each with a InP laser die, a monitor photodetector and a lens, all of which are precion bonded, free of organic compounds, using thin film Au-Sn and other bonding methods. Once the wafer or grid is populated it undergoes a wedge bonding operation and then has a wafer or grid of optically coated silicon lids hermetically sealed onto the die under several atmosphere of helium. The lid is designed with a thinned membrane which serves as an absolute pressure gauge allowing the level of hermeticity to be determined above a threshold value by the bulge of the membrane region. These parts are then tested, diced into separate components, and attached to flex circuitry using BGA attachment. The parts are used to construct recepticalized or pigtailed assemblies for fiber optic transceiver applications such as 10 gigabit Ethernet. This approach allows significant cost reduction, increases thermal and RF performance, allows a very high degree of assembly automation with a simple tool set, significantly reduces part to part variation, and allows substantial size reduction over existing TO cans and hybrid packaging means.

II. Component Characterization

A. Laser Diode Characterization

The characterization of laser diodes using measurements to extract an equivalent circuit has been conducted by numerous researchers, e.g. [7]–[9]. The circuit model from [7], derived by linearizing the rate equations for a laser with a non-uniform lateral carrier distribution, is used successfully to model a laser diode in a 10-Gb/s system [8]. In [9], a butterfly-packaged, 2.5 Gb/s laser module is designed using a similar equivalent circuit extracted from measurement characterization of the laser diode. Using a similar technique, we characterize a

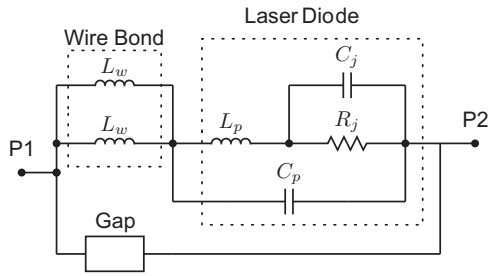


Fig. 2. The circuit model for the measured laser diode is shown consisting of three parts: the S parameters of the gap, the inductances of the wire bonds, and the laser diode equivalent circuit. The computed element values are: R_j=5.9 Ω, C_j=1.2 pF, C_p=0.02 pF, L_p=0.45 nH, and L_w=0.68 nH.

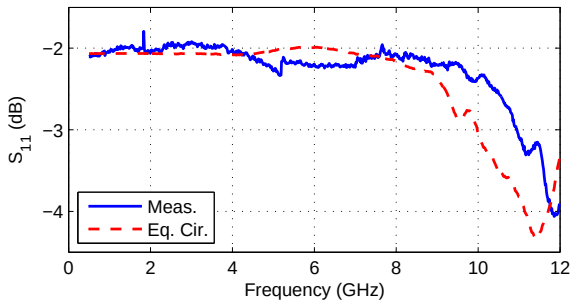


Fig. 3. A comparison of the modeled results using the equivalent circuit compared to the measured results of the laser diode for a fixed bias point of 22 mA. Port 2 (P2) of the circuit in Fig. 2 is virtually grounded for this plot.

1.31-μm Fabry-Pérot directly modulated laser diode designed for 10 Gb/s performance available from Modulight, Inc. The laser diode is measured in series in a two-port configuration with Thru-Reflect-Line (TRL) calibration in 50-Ω microstrip. Measurements of the test circuit without the laser diode give parasitic values for the microstrip series gap that are included in the model. The resulting 2-port data is virtually terminated with a short at port 2 and fit as a 1-port device to the circuit model for the diode shown in Fig. 2. A comparison of the computed circuit model for a 22 mA bias current with the measurement results is shown in Fig. 3.

B. Package Characterization

The silicon package is characterized using Ansoft HFSS. The package design allows for a hermetic seal of the laser and an optically transparent sidewall window with an anti-reflection coating for the 1.31 μm wavelength beam. Signal and monitor lines are routed into the package using hermetic metalized through vias. The initial design, shown in Fig. 1, uses a patterning scheme on the via sidewalls and stripline circuit on the flex substrate for matching. Fig. 1 highlights several of the key challenges of this design. The relative permittivity of the silicon is 11.9, compared to 1.0 for air and 3.5 for the polyamide used for the flex substrate; this wide range of relative permittivity can cause modeling difficulties because of the corresponding range of effective wavelength. In addition, the relative dimensions can cause meshing difficulties: the passivation layer on flex is 18μm thick, which increases the

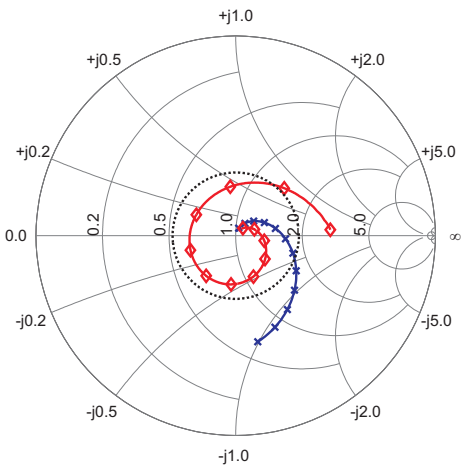


Fig. 4. A comparison of the simulated input match before ('x') and after ('◊') the addition of the impedance matching circuit on the flex substrate. The data are plotted on a 25-Ω Smith Chart with markers at each GHz increment. The 10-dB return loss circle is given.

mesh count; and small metallic features exist on the SiOB in areas that cannot be neglected. These factors, when taken together, create computationally intensive models.

The SiOB is connected to the driver IC with a 2-cm long piece of flexible substrate. This provides stress relief for the connections and room for impedance matching the diode/package combination. The flex substrate is a polyamide, having ϵ_r=3.1-3.5 and $\tan\delta$=0.01-0.04 over the frequency range of interest.

A dual-stub matching circuit is designed on flex to increase the bandwidth of the system. The impedance match of the system with and without the stub-matching compensation on the flex substrate is shown in Fig. 4 on a 25-Ω Smith Chart. The 10-dB return loss circle is given on the graph to highlight the improvement gained with the matching circuit, pushing the 10-dB crossing point from 7.3 GHz to 10.8 GHz.

C. Design Improvements

Three challenges arise from the via configuration for the design described above: the patterning within the vias as shown in Fig. 1(b) adversely affects yield; the via depth is such that parasitic reactances limit performance at high frequencies; and layout or routing of the interconnection is constrained. We investigate an alternate micro-via (MV) design, shown in Fig. 5 The MV design eliminates the patterning within the via (improving yield & high-frequency performance) and eliminates the need for flex stripline matching. This is accomplished by selectively thinning the Si substrate to shorten the vias while preserving mechanical support.

III. System Measurement

Broadband measurements are performed with a Wiltron VNA calibrated with external SOLT standards. A microwave probe with a resistive impedance transformer is used to match the 50-Ω ports of the VNA to the 25-Ω electro-optic driver over

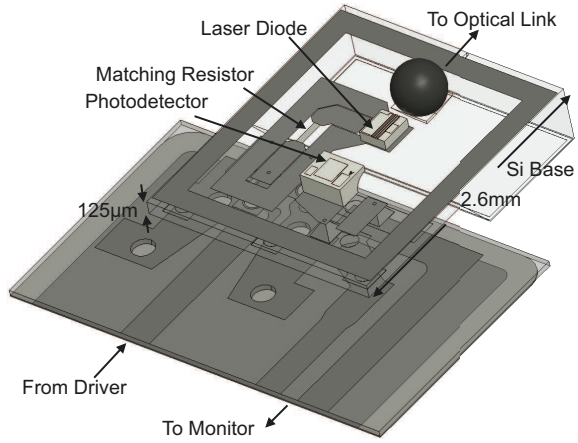


Fig. 5. An annotated sketch of the MV design. For clarity, the Si lid and top passivation layer of the flex substrate have been removed.

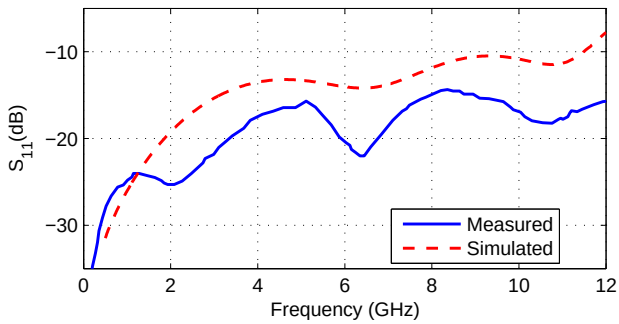


Fig. 6. The frequency response of the system (initial design) showing a comparison of the simulation and measured data. The data are plotted normalized to a 25-Ω reference impedance.

a broad bandwidth. The simulated and measured reflection coefficient for the 10-GHz design is shown in Fig. 6.

The measured and simulated S_{11} response (to 30 GHz) for the MV package is shown in Fig. 7. This does not include the flex circuit. Disagreement between experimental and simulation results above 25 GHz is due to interface differences between the calibration substrate and the SiOB. Subsequent wafers will have integrated calibration standards and more readily accessible test points for 2-port scattering parameter measurements.

In addition to the RF characterization of the system, functional electro-optic testing is conducted on these laser packages. Transmitter optical eye patterns for the system are measured using an Agilent 86100A digital communications analyzer with a 20 GHz optical input O/E converter. The resulting measurements are shown in Fig. 8 for a 10-Gb/s stream of data with a bias current to the laser diode of 45 mA. Measured extinction ratios of both 4 dB are studied for both the initial and MV designs, corresponding respectively to the performance necessary for Ethernet applications.

IV. Extensions to Higher Data Rate Designs

We have presented measured data for two different designs for 10 Gb/s systems. The modules are fabricated using a

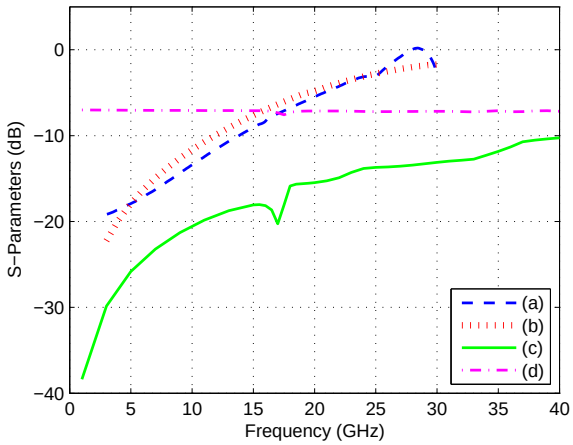
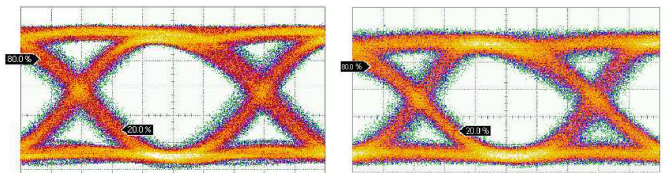
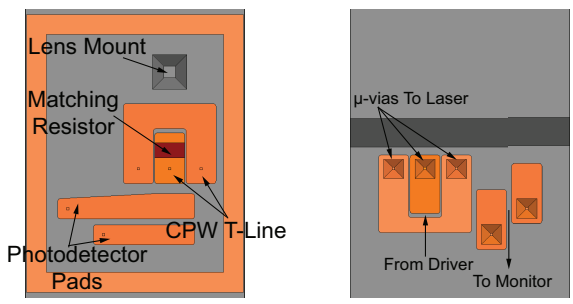


Fig. 7. The frequency response of the system utilizing the MV design, showing a comparison of measured (a) and simulation (b) data. The simulated frequency response of the broadband MV package showing better than 10 dB insertion loss (c), S_{11}, up to 40 GHz, and practically flat transmission (d), S_{21}. These values are close to the theoretical limit near -7 dB due to the series 20-Ω matching resistor. All data are plotted normalized to a 25 Ω port impedance, except port 2 of the broadband design which is normalized to 5 Ω.



(a) (b)

Fig. 8. The eye diagrams for a 10 Gb/s data stream through the package for a 4 dB extinction ratio (a) using the initial design and (b) using the MV design. The horizontal scale on the plots is 16 ps/div.



(a) (b)

Fig. 9. A sketch of the broadband MV package: from above (a), showing the co-planar transmission line (CPW T-Line), and placement of other pertinent features; and from below (b), illustrating how the optimizations simplify the flex substrate designer's task.

parallelized, low-cost approach that provides the requisite system performance. The predictive ability of the modeling techniques have been validated by comparison of the simulated and modeled S_{11} for two design topologies. System-level verification on functional 10 Gb/s optical transmitters provides additional validation of the design process. We have shown that design for performance optimization is possible using the EM simulation tools. By improving the EM performance of the signal lines into the OSA, while maintaining the hermeticity of the packaging, data rates of 25 Gb/s, and potentially data rates of 40 Gb/s, are achievable.

The main areas in which investigation is ongoing to achieve these goals are the following.

1) The development of a straight-through layout of the top-side coplanar waveguide structure.
2) The use of different materials for the matching resistor in order to attain more desirable physical dimensions. The current surface resistivity of the thin-film resistors is approximately 5 Ω/□, which is too low for the resistors to behave as lumped elements in 40-Gb/s systems.
3) Movement of the resistor closer to the laser [4].
4) Optimization of the flex circuit and SiOB interface.

Fig. 7 provides some preliminary simulation results on the new design, illustrated in Fig. 9, indicating that a S_{11} return loss better than 10 dB, and a flat S_{21} response to 40 GHz are feasible.

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