# Design Method for Low-Power, Low Phase Noise Voltage-Controlled Oscillators

Milos Jankovic[#1], Alan Brannon[#2], Jason Breitbarth[*3], Zoya Popovic[#4]

[#]*Department Computer and Electrical Engineering, University of Colorado*
*425 UCB, Boulder, CO, USA*
[1]jankovic@colorado.edu
[2]alan.brannon@colorado.edu
[4]zoya@colorado.edu

[*]*Holzworth Instrumentation, LLC*
*Boulder, CO, USA*
[3]jason@holzworth.com

***Abstract*— This paper presents a design method for voltage controlled oscillators (VCOs) with simultaneous small size, low phase noise, DC power consumption and thermal drift. We show design steps to give good prediction of VCO phase noise and power consumption behavior: (1) measured resonator frequency-dependent parameters; (2) transistor additive phase noise/ noise figure characterization; (3) accurate tuning element model; and (4) bias-dependent model in case of an active load. As an illustration, the design of a 3.4-GHz bipolar transistor VCO with varactor tuning is presented. Oscillator measurements demonstrate low phase noise (-40dBc@100Hz and better than -100dBc@10kHz) with power consumption on the order of a few milliwatts with a circuit footprint smaller than 0.6cm$^2$. The temperature stability is found to be better than +/-10ppm/°C from -40°C to +30°C. The oscillators are implemented using low-cost off-the-shelf surface-mountable components, including a micro-coaxial resonator. The VCO directly modulates the current of a laser diode and demonstrates a short-term stability of $2 \cdot 10^{-10} / \sqrt{\tau}$ when locked to a miniature Rubidium atomic clock.**

## I. Introduction

There are a number of microwave applications that require low-phase noise oscillators. An example of a set of challenging requirements is the case of a chip-scale atomic clock (CSAC) which contains a microwave voltage-controlled oscillator (VCO) which locks to the atomic resonance of alkali atoms, such as Rubidium. When the entire miniature atomic clock needs to be in a 1-cm$^3$, 30-mW package [1], a large fraction of the power is dedicated to thermal management and locking [2],[3], leaving a small power budget for the VCO. To be comparable in stability with existing compact atomic frequency references, fractional frequency instability below $10^{-11}$ is required at one-hour integration times and longer [2].

The requirements for this new technology are pushing the state-of-the art in oscillator design to develop a local oscillator (LO) that exhibit combined lower phase noise, less power consumption, and smaller size than previously published voltage-controlled oscillators. To effectively modulate the laser light field, the LO frequency must be either exactly equal to or half of the hyperfine ground-state splitting frequency for Rubidium (or Cesium) atoms and tunable to compensate for frequency differences due to temperature, part tolerances, and other variables. Designing for half of the hyperfine splitting frequency, a VCO is needed at 3.417GHz for Rb.

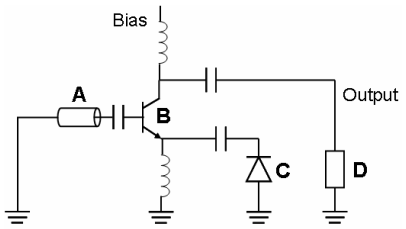


Fig. 1 Simplified schematic of a VCO. The transistor (B) is shown as a bipolar device, and the tuning element is a diode (C). The resonator (A) is connected to the input terminal of the transistor while the load (D) can be active and is connected to the output terminal. The bias line is not assumed to be an ideal choke.

In this paper, we discuss the design and the experimental validation of the design method for low-phase noise and low-power consumption VCOs designed for a very specific and precise frequency and output power while simultaneously satisfying tight volume constraints. We show that the method can be applied effectively for design of VCOs that meet requirements for challenging applications such as CSAC.

## II. Experimentally-based Oscillator Design Method

When designing the VCO, and in reference to Fig.1, the oscillator circuit is divided as follows: (A) resonator, including coupling to the circuit; (B) transistor and biasing circuit; (C) tuning element and coupling to the circuit; and (D) load and its bias-dependent properties. All four elements need to be independently characterized for a successful prediction of final oscillator design behavior.

### *A. Resonator Selection*

Generally, when very small size, microwave frequency and high Q are of interest, the following choices for resonators are: research-level quartz crystals, coaxial resonators, MEMS mechanical resonators, and recently designed bulk acoustic resonators [4]. In the example presented here, a λ/4 ceramic-

filled coaxial resonator as in [5] is chosen because of its high Q, small size (2mm by 2mm by 3.9mm for 3.4GHz) and good thermal stability (+7ppm/°C, with other values available). Such resonators have more than three times better stability over wide temperature variations than recently produced high-Q film bulk acoustic resonators (FBARs) [6]. Despite the relatively low cost of the surface-mount coaxial resonators (several dollars per resonator), it remains the most expensive component of the microwave oscillator.

The resonator is a ceramic-filled square coaxial quarter-wavelength transmission line which is modeled as a parallel RLC circuit at self-resonance. When used below resonance and coupled capacitively to the rest of the circuit, the resonator becomes a series RLC circuit. The unloaded Q is measured to be $Q_0$=210 at self-resonance [7]. If the Q factor is sufficiently high, the magnitude of the input impedance bandwidth gives a reasonable estimate. With a dielectric constant of 37.4, a characteristic impedance of 9.2Ω, and an outside diameter of 2.0mm, the inside diameter was calculated to be 0.787mm for a circular coaxial transmission line model in Agilent's ADS software. The length of the line was adjusted to match measured resonance data.

The thermal frequency drift of the coupled resonator was measured with a simple op-amp feedback circuit, a power resistor (heat source) and a thermistor (for measurement) affixed to the brass plate. While the frequency shift with temperature is specified by the manufacturer as +7±2ppm/°C, the overall frequency shift was found to vary from approximately -6ppm/°C near room temperature to -13ppm/°C at higher temperatures, most likely due to the thermal coefficient of the series capacitor. (a Panasonic series ECD multilayer ceramic capacitor with a C0G temperature coefficient of 0±30ppm/°C).

### *B. Transistor Noise Characterization*

One of the parameters that can aid in predicting the final oscillator phase noise is the transistor noise figure (NF) [8, 9], which is given in most manufacturers' data sheets, but is measured at small signal levels. In oscillators, transistors operate in large signal mode, usually 2-3dB in compression. In [10], it is experimentally shown that many amplifiers exhibit an increase in broadband noise of 1 to 5 dB as the input signal increases, and the NF in terms of single-sideband phase-modulation noise is given by

$$L(f) = N_{th}+NF-P_{in}$$

where $N_{th}$ is the room temperature thermal noise and is equal to -177dBm, $P_{in}$ is the signal power in dBm and $L(f)$ is the PM noise in dBc/Hz and corresponds to the wideband PM noise floor of an amplifier. From here, the oscillator phase noise can be found using the following equation [10]:

$$L(f_m)=10\log_{10}\left[\left(\frac{F\cdot kT}{2\cdot P_{in}}\right)\cdot\left(1+\frac{f_0^2}{(2\cdot f_m\cdot Q_{loaded})^2}\right)\cdot\left(1+\frac{f_c}{f_m}\right)\right]$$

where $f_0$ is the carrier frequency, $L(f_m)$ is the ratio of the phase noise in a 1Hz bandwidth to the common oscillator output level, $f_m$ is the carrier frequency offset, $f_c$ is the noise edge of the $1/f$ noise of the oscillator, and F is the noise figure.

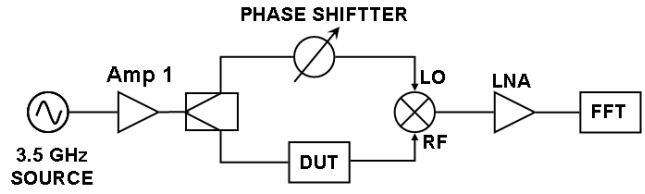


Fig. 2 Block diagram of a 3.5GHz additive phase noise measurement system.

A large-signal noise figure measurement can be used to find the additive phase noise of an amplifier or the phase noise of an oscillator using a given device at a given bias point. To ensure that the noise contribution of the additive phase noise measurement system shown in Fig. 2 is much lower than the PM noise of the transistor under test, a very clean source at 3.5GHz is developed. The output of a 100-MHz oven-controlled crystal oscillator is amplified and then up-converted using a low phase-noise comb-generator nonlinear transmission line (NLTL) multiplier. The 500-MHz signal component is filtered, amplified and multiplied through another NLTL which generates the required 3.5-GHz source signal in Fig. 2. The phase shifter establishes phase quadrature between the two signals at the mixer inputs. The amplified mixer output is detected and is converted as additive phase noise of the DUT by a Stanford Research Systems SR760 FFT spectrum analyzer. The system provides a noise floor of -168dBc/Hz at 100kHz offset from the carrier. Once the additive phase noise $L(f)$ of a transistor is measured, using e.(1), the large-signal NF of the device is determined. The measurement also gives information about the flicker ($1/f$) noise of the transistor in the amplifier circuit.

As an example, the results are given in Fig. 3 for three different bipolar transistors connected to 50-ohm input-output lines, with grounded emitters and with 20-kΩ base bias resistors. The measurement system noise floor is sufficiently low for measurement validity. The last data point, at 100kHz offset, is considered to be the thermal noise level $L(f)$ and the NF of the transistor is calculated from $177+P_{in}+L(f)$ [10].

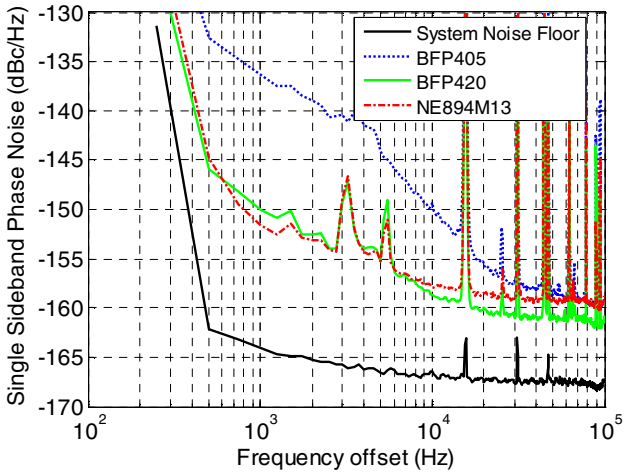


Fig. 3 Additive phase noise measurements for three BJTs (Infineon BFP405 and BFP420 and CEL NE894M13) at a collector bias of 2.5V and for Pin = -10dBm.

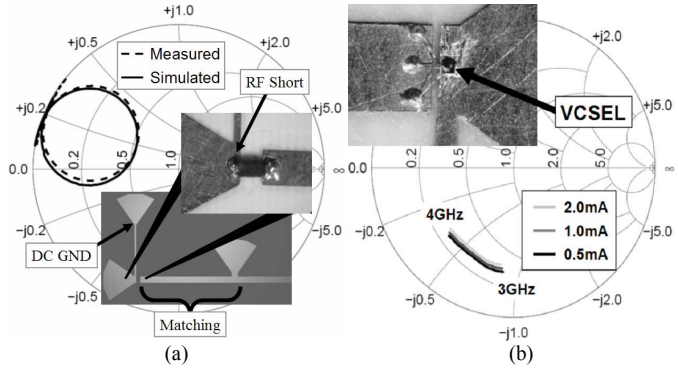


Fig. 4 (a) Photograph inset show shows 1SV280 varactor and its location in a test circuit, as well as measured and simulated varactor impedance used in developing an equivalent circuit model. (b) Photograph of the VCSEL wirebonded to its test circuit and measured input impedance versus bias current and frequency from 3GHz to 4GHz.

### C. Tuning Element Characterization

In the example application a narrow tuning range of around 3MHz is desired to give better frequency precision [5]. A weakly-coupled varactor diode (MA-COM MA46505) provides tunability, Fig. 4. The diode location in the circuit permits a variable phase shift due to the changing capacitance. It is important that the varactor diode be modeled correctly at the oscillation frequency, since the junction capacitance $C_j$ and the series resistance $R_S$ are often specified at 50MHz, but vary significantly with frequency. The technique is similar to that presented by [11] in which the equivalent circuit model at 50MHz, taken from the datasheet, is matched to 50Ω at the frequency of interest. Because the accuracy of a network analyzer is typically ±0.05dB, and a typical varactor series resistance is one or two ohms, there are significant errors if the varactor impedance is measured directly. The goal is to move the measured impedance closer to the center of the Smith chart where calibration errors have little effect. We have modified the technique in [11] to obviate the need for vias for RF and DC ground because the microstrip lines and radial stubs are more reliably modeled with planar EM software. The RF short was validated by a separate experiment; if the measured RF impedance at the point marked "RF Short" in Fig. 4 is not a true RF short circuit, then the measured S parameters of this section are included in the model. The same is true for the radial stub that forms part of the matching circuit shown in Fig. 4. Following this approach, a series resistance greater than 2Ω at 3.4GHz was found, with the actual value varying based on bias voltage.

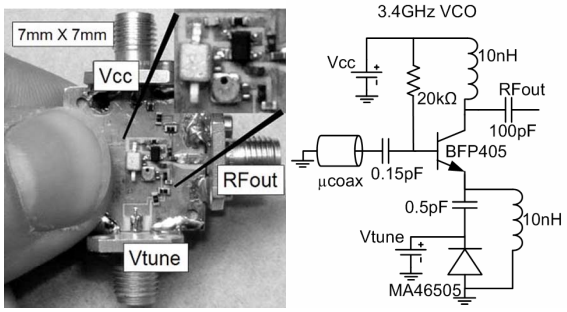


Fig. 5 Photograph and circuit diagram of the 3.4GHz VCO. The inset shows the actual footprint of the oscillator, 0.6cm$^2$.

### D. Active Load Characterization

The load for the oscillator output in the atomic clock is a vertical-cavity, surface-emitting laser (VCSEL) that is tuned to an optical absorption frequency of 795nm for Rb. This load was measured under several bias conditions, with the VCSEL mounted in a microstrip circuit, Fig. 4. The circuit was calibrated with TRL standards and the reference plane set at the end of the microstrip line before the wirebonds. Fig. 4 shows the resulting measured RF impedance of a 795nm VCSEL at different bias conditions over a frequency range of 3GHz to 4GHz. The nominal impedance at 3.4GHz is 16-j31.6Ω. The output of the VCO can be designed directly for this load impedance to eliminate extra matching circuitry.

### E. Electrical and Thermal Circuit Modeling

The feedback characteristics of the oscillator were modeled similarly to [12], using Agilent ADS harmonic balance simulations. The lumped elements are modeled with equivalent circuits given by the manufacturers, while the resonator, varactor and transistor are modeled as described previously. The oscillator presented here is not matched to this impedance due to the unknown final package and length of transmission line to the VCSEL.

To a first approximation, the expected thermal frequency drift is calculated based on the loaded system Q and the thermal phase shift of the transistor. The oscillator loaded Q is given by $Q = (\omega/2)\cdot(\partial\phi/\partial\omega)$, where $\omega$ is the frequency of oscillation and $\phi$ is the phase of the output waveform. Considering a critically coupled system with a loaded Q of approximately 100, we express the ratio of the rate of phase change to the rate of frequency shift as

$$\left.\frac{\partial\phi}{\partial\omega}\right|_{Q=100} = 6.923\cdot10^{-9} \qquad (2)$$

The simulated phase change at 25°C is 0.69064 rad, and the simulated phase change at 35°C is 0.68838 rad, resulting in a phase shift per °C due to the transistor of -0.000226 rad/°C. Substituting the expected system phase shift into (2), we have

$$\partial\omega \approx \frac{\Delta\phi_{BJT}}{6.923\cdot10^{-9}} = -32.6\text{kHz}/^{\circ}\text{C}$$

which results in a -7ppm/°C frequency drift due to the transistor. This result was used to select the +7ppm/°C temperature coefficient for the resonator, which influenced the choice of dielectric filling.

## III. Oscillator Characterization

The power necessary to optimally modulate the VCSEL in the Rubidium-based CSAC at NIST is approximately -6dBm, when delivered into a 50-Ω load [5]. Fig.5 shows a photograph and detailed circuit diagram of the fabricated 3.4GHz VCO. The measured RF output power level ranges

from -16 to 2dBm as the power consumption is from 1 to 7.6mW, respectively.

The phase noise of the 3.4GHz VCO was measured out to a 100-kHz offset. The 3.4GHz oscillator is measured at a bias voltage of 1.3V and shows little degradation as the bias is decreased to 1.1V. As shown in Fig. 6, the phase noise measured at a 10-kHz offset is -102dBc/Hz. The close-in phase noise is -42dBc/Hz at a 100-Hz offset. These results are better than the current expected phase noise requirement of -25dBc/Hz at 100-Hz offset [5]. The VCO was cycled between -40°C and +70°C in a temperature chamber. Over the range of -40°C to 25°C, the oscillator exhibits less than 1MHz of frequency change, representing an average thermal drift less than ±10ppm/°C.

To demonstrate sufficient quality for application in chip-scale atomic clocks, the VCOs have been locked to the hyperfine splitting frequency of Rubidium atoms at the National Institute of Standards and Technology (NIST) in Boulder, CO. For these measurements, a setup was used similar to the one in [5] designed to mimic that used by future chip-scale atomic clocks. The measured fractional frequency instabilities of the locked oscillator is shown in Fig.7. The VCO has been locked to the atomic resonance by the large increase in stability, reaching a value of $10^{-11}$ at approximately 200 seconds. Due to long-term thermal drift of the atoms and physics package, the stability degrades at longer times.

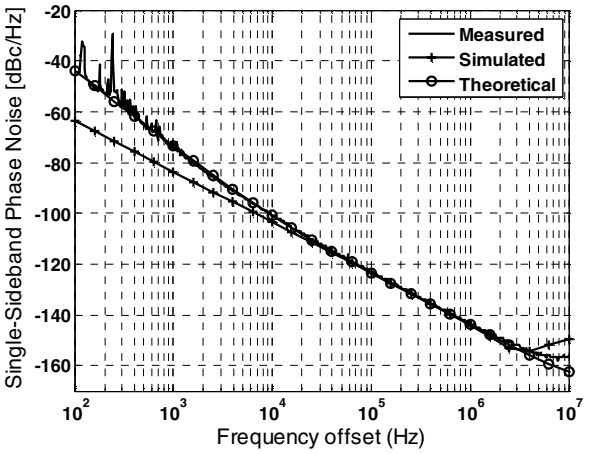


Fig. 6 Measured, simulated and theoretical phase noise for the 3.4GHz LO. The measured data were only taken to a maximum offset frequency of 100kHz. The theoretical plot is obtained from measurements and Eq.(1).

In summary, we have presented a design procedure for design of low-phase noise oscillators with simultaneous small size and low power. The experimental example has applications in miniature low-power atomic clocks.

## ACKNOWLEDGMENT

This work was funded by the DARPA CSAC program, under subcontracts to the University of Colorado from Teledyne and NIST. The authors are grateful to Val Jackson of Val Jackson & Associates, Inc. for samples and technical advice on the coaxial ceramic resonators, and to Roy Berquist at Rockwell Collins in Cedar Rapids, IA for help with measurements in the temperature chamber. The authors express thanks to Dr. John Kitching, Dr. Peter Schwindt, Dr. Vladislav Gerginov, and Vishal Shah from NIST for their successful efforts to lock our oscillators to their atomic physics setup.

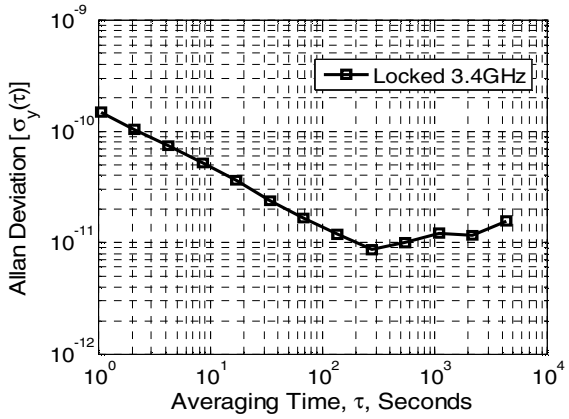


Fig. 7 Measured frequency instability of the VCOs locked to the atomic resonance of Rb atoms. The data show a significant improvement over the instability requirement, expected to be $6 \cdot 10^{-10}$ at 1sec integration time.

## REFERENCES

[1] V. Gerginov, S. Knappe, P.D.D. Schwindt, V. Shah, L. Liew, J. Moreland, H. G. Robinson, A. Brannon, J. Breitbarth, Z. Popovic, L. Hollberg, J. Kitching, "Component level demonstration of a micro-fabricated atomic frequency reference." *Proc. of the IEEE Joint Intnl. FCS and PTTI Systems and Applications Meeting*, pp. 758-766, 2005.

[2] S. Knappe, V. Shah, P.D.D Schwindt, L. Hollberg, J.Kitching, L.A. Liew, and J. Moreland, "A microfabricated atomic clock," *Applied Physics Letters*, vol. 85, pp. 1460-1462, 2004.

[3] R..Lutwak, Pl. Vlitas, M. Varghese, M. Mescher, D.K. Serkland, and G.M. Peake, "The MAC – a miniature atomic clock," in *Joint Meeting of the IEEE Intern. Freq. Control Symp. and the PTTI Systems and Applications Meeting*, Vancouver, Canada, 2005.

[4] Svenja Knappe, Chapter Emerging Topics: MEMS Atomic Clocks; in Comprehensive Micro-systems, Eds. Yogesh Gianchandani, Osamu Tabata, Hans Zappe, Elsevier, Amsterdam, in press, 2007

[5] A. Brannon, J. Breitbarth, Z. Popovic, "A low-power, low phase noise local oscillator for chip-scale atomic clocks," *2005 IEEE MTT-S IMS Digest*, vol. 12-17, pp. 1535-1538, June 2005.

[6] A. P. S. Khanna, *et al.* "A 2GHz voltage tunable FBAR oscillator," *2003 IEEE MTT-S IMS Digest.*, vol. 2, pp. 717-720, June 2003.

[7] D. Kajfez and E.J. Hwan, "Q-factor measurement with network analyzer," *IEEE Trans. Microwave Theory Tech*., vol. MTT-32, pp. 666-670, July 1984.

[8] L. S. Culter and C. L. Searle, "Some Aspects of the Theory and Measurement of Frequency Fluctuations in Frequency Standards," *Proc. of IEEE*, vol. 54, no.2, pp.136-154, Feb 1966.

[9] D. B. Leeson, "A simple Model Of Feedback Oscillator Noise spectrum," *Proceedings Letters*, pp.329-330, February 1966.

[10] A. Haiti, D. A. Howe, F. L. Walls, D. Walker, "Noise Figure vs. PM Noise Measurements: A Study at Microwave Frequencies," *Proc. 2003 IEEE Int. Freq. Control Symp.*, pp.516-520, 2003.

[11] G. H. Stauffer, "Finding the lumped element varactor diode model," *High Freq Electronics*, Summit Technical Media, 2003.

[12] S. Alechno, "Analysis method characterizes microwave oscillators, 4-part series" *Microwaves & RF*, vol. 36, pp. 82-86, Nov.1997-1998