MINIATURE 3D MICRO-MACHINED
SOLID STATE POWER AMPLIFIERS

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Introduction

Conventional solid state power amplifiers [SSPAs] usually employ a mix of Monolithic Microwave Integrated Circuits [MMICs] and passive microstrip circuitry which include chip components and wire bonds, usually assembled on a ceramic or similar substrate. Microstrip or coplanar waveguide (CPW) transmission lines realized with thin or thick film metallization is used for electrical interconnect. Such hybrid microwave circuits have been built for decades and remain the dominant method to combine MMICs into a module. In this work, we replace the microstrip with a rectangular coaxial transmission line created by sequential photolithography and plating processes, resulting in a very wide band, dispersion-less transmission medium which includes integrated passive components. This approach yields a number of advantages over conventional microstrip circuits:

- A 250-um square coax is purely TEM up to ~450GHz [1], resulting in low dispersion and enabling broadband components;
- Since components are defined photolithographically in two dimensions, and by sequential growth and polishing in the third dimension, exacting tolerances can be maintained, lowering manufacturing costs and improving overall performance;
- Low insertion loss (0.08dB/cm measured at 38GHz) provides a means for high power combining efficiency;
- Fully enclosed signal path results in high isolation between neighboring lines enabling dense multilayer circuits.

This 3D micro-machining technology, called Polystrata™ technology, in which the circuit is the package, and the package is the circuit, enables one other important and far reaching advantage. Consider that in a typical power MMIC, the active transistor generally occupies < 5% of the total chip area, the remainder of which is composed of transmission lines and passive structures, as illustrated in
Fig.1. For a technology where a single wafer can cost $30,000 or more, a hybrid integration rather than monolithic integration is not only enabling, but revolutionary in its implications. The Polystrata technology platform enables a completely new class of “MMIC-less” architecture, enabling rapid prototyping for new applications and low cost power amplifiers, leveraging traditional silicon fabrication and MEMS processes.

**Polystrata Fabrication Process**

Polystrata microfabrication technology allows for the manufacture of air-dielectric metal RF backplanes and provides a unique combination of features:

1) It allows microwave signals to be routed in three dimensions with very little loss over a wide frequency band;
2) It prevents cross-talk between directly adjacent lines;
3) It is formed in copper and can therefore dissipate substantial amounts of heat;
4) It is capable of creating passive microwave elements such as splitters, combiners, filters, resonators, antenna, and so on as part of the manufacturing process.

**Figure 1.** Wideband Power MMIC - The active transistors, shown in red, occupy only ~2% of the total chip area. Chip size is approximately 8 mm x 8 mm.

**Figure 2.** Rendering of a recta-coaxial transmission line implemented with a Polystrata process having 5 stratum. The photomicrograph in the background shows transmission lines and test structures.

Recta-coax lines and components are fabricated using a sequential microfabrication process described in [2] and depicted in Fig.2. Similar to surface micromachining techniques, the recta-coax structures are built up layer by layer by depositing a uniform copper stratum, and sequence of strata comprised of photo-resist and copper. In the 5-layer coax depicted in Fig. 2, a dielectric polymer supporting the center conductor is a part of the 3rd layer. The total height of the 5 layer structure is approximately 300 μm. Once the structure is fabricated, the resist is drained through release holes in the top and side walls. The structure
is built on either low or high-resistivity Si wafers; however, other substrates may also be used. It is possible to fabricate micro-coaxial lines with more than 5 layers, and some 11-layer designs are presented in [6, 7].

**Passive Component Design and Modeling**

Three types of passive structures have been designed and implemented with Polystrata microfabrication technology:

1) Passive *elements*, such as lumped inductors, various transitions, lines of impedances varying between 8 and 90 ohms, standardized chip sockets for surface-mount integration, etc., which are building blocks for other higher level components. Theoretical considerations for basic line properties are given in [1], and these include effects of fabrication uncertainties;

2) Passive stand-alone *components*, such as quasi-planar resonators [3, 6], branch-line couplers [4, 5, 7], Wilkinson combiners/dividers, Lange combiners/dividers, low-pass filters, resonant cavities, patch antennas [5] and coaxial impedance transformers;

3) Passive *networks* (circuits) including divider/combiner, bias, and matching circuits which are intended for integration with active elements.

Next, we provide some detail on a few of the components listed above. One of the advantages of the Polystrata technology is the wide available range of characteristic impedances for the coaxial lines. Fig.3 shows an example of an 11-strata cross-section and simulated range of characteristic impedances as the dimensions of the line vary within allowed fabrication parameters.

![Figure 3](image)

*Figure 3.* Simulated characteristic impedance range possible with 11-layer lines formed with the Polystrata process, as a function of width of inner conductor for a 500-um width of rectangular cross-section outer conductor.
Other interesting examples of components that have been fabricated using this technology are shown in Figs. 4 and 5, and details can be found in [3-7]. Fig. 5 shows air-filled copper Ka-band resonators with and without loading inside the cavity. These quasi-planar components with heights between 250 and 700 μm are demonstrated with measured unloaded Q factors between 440 and 830, respectively. Miniaturization of up to 70% in footprint area with respect to a TE101 quasi-planar resonator is accomplished by low-loss loading, and finite-element simulations predict the measured resonant frequency within less than 1%.

![Figure 4](image1.png)  
**Figure 4.** (a) An SEM image of a 10-dB directional coupler fabricated using micro-rectangular coax designed for operation centered around 26 GHz. The naming convention for the ports is labeled and an insert of the model used for simulating the design is shown in the bottom right corner. (b) Simulated (dotted) versus measured (solid) S parameters for a 10-dB coupled-line directional coupler designed for operation centered around 26 GHz.

![Figure 5](image2.png)  
**Figure 5.** (a) Photographs of two cavity resonators with Q~800 fabricated for operation at 36GHz. The resonator at left, R1, is full-sized, and the resonator at right, R2, uses miniaturization. The release hole size is 400 by 400 μm. Probing of the structure is done on the ends of the resonator at ports indicated by P1 and P2.

**Chip Integration**

Polystrata technology is ideally suited for addressing two problems that can limit the performance of conventional hybrid circuits: bond wire parasitics and thermal

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management. In addition, instead of being limited by lumped element values and properties dictated by monolithic fabrication, the designer can choose the best SMT component to be mounted in a Polystrata standard device socket for optimal performance while not sacrificing cost. Sockets have been designed for standard 0402, 0303 and other surface mount packages.

Active devices can also be embedded directly into Polystrata lines. Fig.6 shows an embedded architecture approach in which a discrete active device is directly flip-chip assembled into an active Polystrata device socket with bias lines included as two-wire rectangular lines. The performance of the chip (in this case an amplifier) is indistinguishable from the small-signal performance measured on-wafer for the same active device. The agreement between the on-wafer and in-Polystrata device measured $S_{21}$ parameter for this device between 1 and 10GHz confirms the excellent control of parasitic reactance that is achievable with the Polystrata design.

![Bias line](image)

50-Ω port

(a) (b)

Figure 6. (a) Un-populated active Polystrata device socket, showing 50-ohm input and output ports and drain and gate bias lines, prior to flip-chip assembly. (b) Photograph of an amplifier chip flip-chip assembled with silver epoxy onto an active Polystrata socket. (c) Measured small-signal $S_{21}$ performance of chip on wafer and (d) in the Polystrata reacta-coax environment for several different devices.

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Results and Conclusions

In addition to dense integration, ability to combine high-quality components, wafer scale fabrication, reduced cost of active device area, low loss, low dispersion, and very high isolation, the Polystrata reacta-coax environment also provides a relatively high-power medium and good heat sinking. The former is facilitated by coaxial line design and the latter by the virtue of using copper as the conductor with minimal volume of low-thermal conductivity dielectrics. In the case of active devices, one can envision a unique copper cap that facilitates two sided heat-sinking for thermal management. This approach is a topic of current research and simulations show that it results in:

- Controlled parasitic reactances and resistances – precision interconnect design
- Compatibility with micron-precision bonding – die bonder compatible assembly;
- Compatibility with fluxless, thin-film solder- Au/Sn thin film eutectics at 5 µm thickness;
- Double-sided heat sinking – Heat is removed from both side of active die; and
- Capability for rework – a “chips last” process allows die to be removed.

A number of additional components that are difficult to integrate and miniaturize in microstrip hybrid or MMIC environments are illustrated by a block diagram of a power-combining power amplifier as shown in Fig.7. The amplifier includes broadband divider-combiner networks, bias tee networks, matching circuits, active device sockets, and the important transitions to standard connectors to enable insertion into existing systems. A 20-W version of this type of amplifier with a 4:1 frequency bandwidth is the topic of current research.

![Figure 7](image)

**Figure 7.** Block diagram of a power-combining PA that is the topic of current research. Polystrata active device pair sockets, bias lines, matching networks and divider/combiner networks are designed for a 4:1 frequency bandwidth and 20-W power handling capability. CPW-microcoax interconnects are developed for transitions to standard connectors.

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References


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