A 65–W High–Efficiency UHF GaN Power Amplifier

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***Abstract*— This paper presents a high–efficiency UHF power amplifier (PA) using a GaN HEMT on a SiC substrate transistor as the active device. The PA delivers 65 W with 82% power added efficiency (PAE), and 45 W with 84% PAE at 370 MHz, with supply voltages of 35 V and 28 V, respectively. Load pull techniques under Class–E conditions are used for device characterization and matching network design. The PA is implemented in a hybrid circuit with mixed lumped–element and transmission–line matching networks. A weighted Euclidean distance is defined to enable tradeoff studies between output power (P_{OUT}) and efficiency, in order to find the final optimal amplifier design.**

***Index Terms*— GaN HEMT, High–Efficiency, Class–E, UHF, Power Amplifiers**

I. INTRODUCTION

STATE–of–the–art wide–bandgap semiconductor RF transistors are delivering record–breaking power levels from solid–state devices at microwave frequencies. Some of the commercial transistors can deliver more than 20 W of output power with cutoff frequencies higher than 3 GHz. A number of excellent amplifiers have been demonstrated in the lower microwave frequency range [1]–[4].

The UHF region can also benefit from these novel devices [5]. Wide–bandgap semiconductors have better intrinsic material properties compared to standard Si LDMOS transistors, i.e. larger energy gap (support higher internal electric fields before breakdown), lower dielectric value (lower capacitive loading), higher thermal conductivity (higher heat handling), and higher critical electric fields (higher RF power) [6]. High voltage operation and high power density with low parasitic reactance translate into robust devices that can withstand high–stress conditions typically associated with switched–mode operation. For example, in Class–E mode the peak voltage across the device can be more than 3.56 times higher than the supply voltage [8]. The supply voltage must then be limited by this factor ($V_{\mathrm{DSS}}/3.56$ where V_{DSS} is the absolute maximum drain-to-source voltage). Therefore, devices with high breakdown voltage are ideal for this mode of operation.

In this paper, a high–efficiency high–power UHF transmission line Class–E power amplifier is designed with a GaN HEMT on a SiC substrate transistor from RFMD that is able to deliver 60 W in the 2 GHz range when operated in Class–AB mode with a 48 V supply. Loadpull techniques under Class–E conditions are used for device characterization. A weighted Euclidean distance is used to assess the tradeoff between output power and efficiency for the final optimal amplifier design. Figure 1(a) shows a picture of the final Class–E PA, while Figure 1(b) shows a power sweep for a supply voltage of 28 V.

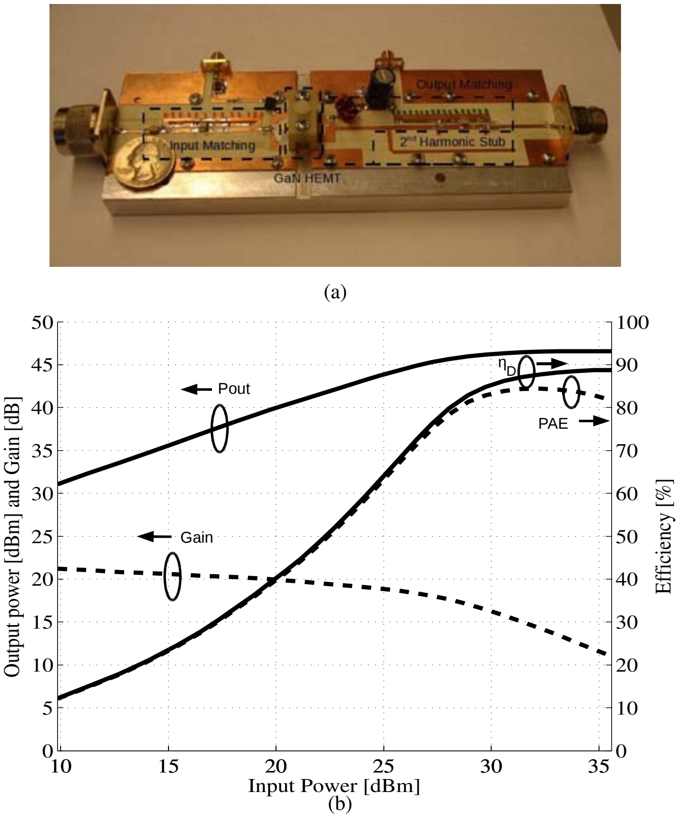

Fig. 1. A photograph of the final hybrid transmission line class-E PA. (b) Input power sweep of the class-E mode 370-MHz PA for a supply voltage of 28 V. The maximum PAE is 84% with a drain efficiency of 87% and 45 W of output power.

II. HYBRID CLASS–E AMPLIFIER

In Class–E operation the transistor behaves as a switch. The device is biased close to cutoff and driven into compression. The transistor turns ON and OFF with the RF drive which also provides the switching frequency. For the device to operate in ideal Class–E, all the harmonics must be terminated in an

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open circuit, while the fundamental is matched to the Class–E impedance which depends on the operating frequency and the device intrinsic output capacitance [7]-[13]. Class–E power amplifiers have been shown to achieve efficiencies in the order of 95% in the low MHz range and 70% at X–Band ([10], [11], [1], [12]).

In the transmission line Class–E implementation an open stub offers a high–impedance termination at the second harmonic [9]. Additional harmonics can be terminated for small improvements in efficiency at the expense of circuit complexity. The fundamental Class–E impedance can be estimated from the transistor output capacitance and the operating frequency. The output capacitance can be approximated from the linear S-parameters of the device and in our case is close to 9 pF. The Class–E impedance is calculated to be $9 + j10\,\Omega$ at 370 MHz.

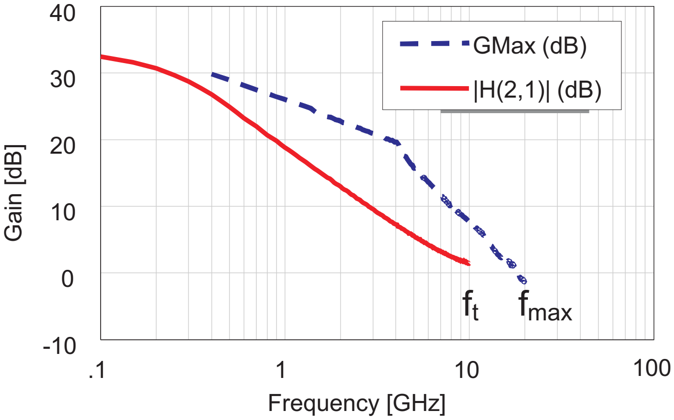

Fig. 2. Short circuit current gain and maximum available gain of a 0.5 μm gate length GaN HEMT with source coupled field plate.

AlGaN/GaN HEMTs based on an RFMD developed process are used as the active device [14]. These transistors are fabricated on a 3-inch silicon carbide (SiC) substrate for improved thermal dissipation performance at increased power density over existing semiconductor technologies. The process gate length is 0.5 μm, and additionally employs source connected field modulation plates, which allow operation at a quiescent drain voltage of up to 50 V. This high operating voltage increases the device optimum impedance and lowers the device output parasitic capacitance for a given output power capability. The devices exhibit a pinch–off voltage of about -4 V and a peak current density of 0.9 A/mm. The current and power gain cut–off frequencies (f_t and f_{max}) as measured from small periphery devices are 11 GHz and 18 GHz (Figure 2), respectively, at a drain voltage of 48 V with a low Class-AB bias point of 20 mA/mm. Pulsed measurements on $2 \times 400\,\mu$m AlGaN/GaN HEMT devices typically provide a saturated output power density greater than 3 W/mm at a drain voltage of 28 V and a saturated output power density greater than 5 W/mm at a drain voltage of 48 V.

The Class–E amplifier is fabricated on a 0.762 mm thick Rogers RO4350B substrate. The matching networks are implemented as a hybrid between transmission line and lumped components as shown in Figure 1(a).

III. TRANSISTOR CHARACTERIZATION

Load pull techniques can be used as a robust empirical method for characterizing transistors for Class–E operation by including the harmonic termination in the test fixture. Focus Microwaves load pull automatic tuners are used to obtain output power and drain efficiency contours at the operating frequency. The transistor is mounted in a modular fixture that allows TRL calibration placing the reference planes at the device leads.

The transistor was characterized at 370–MHz under three different supply voltages; 28 V, 36 V and 48 V and the results are shown in Figure 3. Figure 3(a) shows P_{OUT} and η_{D} contours for a 28 V supply voltage. The Class–E impedance predicted by the simple theoretical formulae, e.g. [13] with a 9 pF device output capacitance is marked '*' for comparison. From the figure it can be observed that the optimal output power and drain efficiency contours do not overlap. This means that a tradeoff analysis is necessary in order to choose the amplifier output impedance matching. Ultimately, the PA designer needs to deal with this analysis depending on the particular application. However, the next section discussed a proposed optimization procedure based on a weighted Euclidean distance.

Figure 3(b) shows the output power trend as a function of supply voltage. As the drain voltage increases the optimal impedance imaginary part increases toward higher inductance, while the real part remains approximately constant. Figure 3(c) shows that the optimum drain efficiency remains constant. Assuming no varactor effect in the output capacitance the Class–E impedance should remain constant as a function of supply voltage, since the supply voltage only scales the amplitude of the voltage and current waveforms across the device but does not change their shape.

IV. OPTIMUM LOAD IMPEDANCE SELECTION

It can be seen from the example in Figure 3(a) that a load impedance matching that optimizes power is not the same as the impedance matching that optimizes efficiency. For a particular PA design it would be useful to have a guideline of how much output power needs to be sacrificed to meet a particular efficiency specification. In this section we propose a simple method which allow a systematic approach to this tradeoff.

The method is outlined as follows:

- For each impedance the measured output power versus measured efficiency is plotted from load pull data. An example is given in Figure 4.
- Given that the data deviates significantly from a straight line we defined the metric "h" as the Euclidean distance from the origin.
- If this metric is defined in terms of output power and efficiency the metric is as follows,

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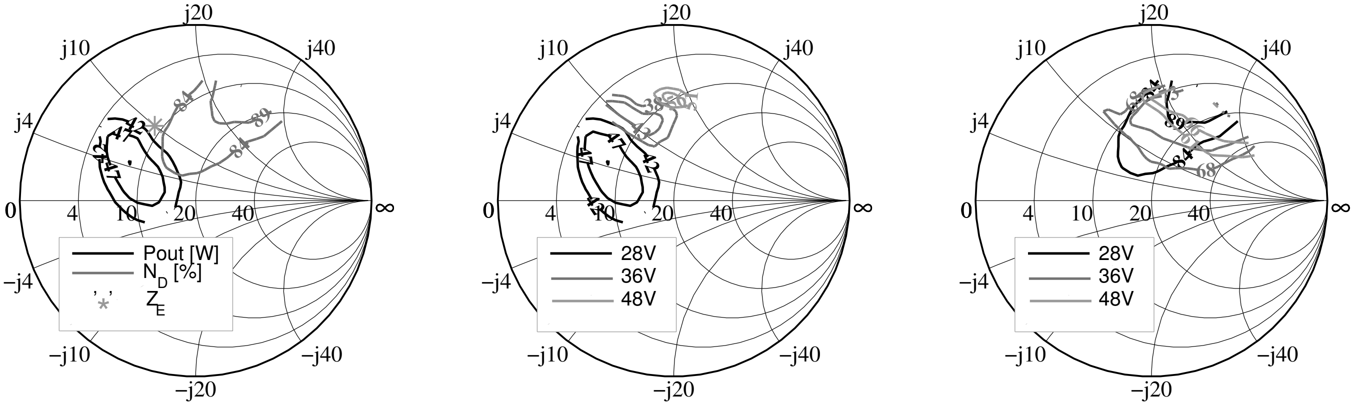


(a) (b) (c)

Fig. 3. Load pull contours for the RFMD GaN HEMT on a SiC substrate. (a) P_{OUT} (W) and η_{D} (%) contours when the transistor is biased at 28 V. The optimum P_{OUT} and η_{D} regions do not overlap. The figure also shows the optimal Class–E impedance $(9 + j10\,\Omega)$ estimated from the device 9 pF output capacitance marked with '*'. (b) P_{OUT} (W) and (c) η_{D} (%) contours when the transistor supply voltage is 28 V, 36 V and 48 V. The optimal output power impedance varies as a function of the supply voltage, while the high efficiency region remains constant. The Smith charts are normalized to 20 Ω.

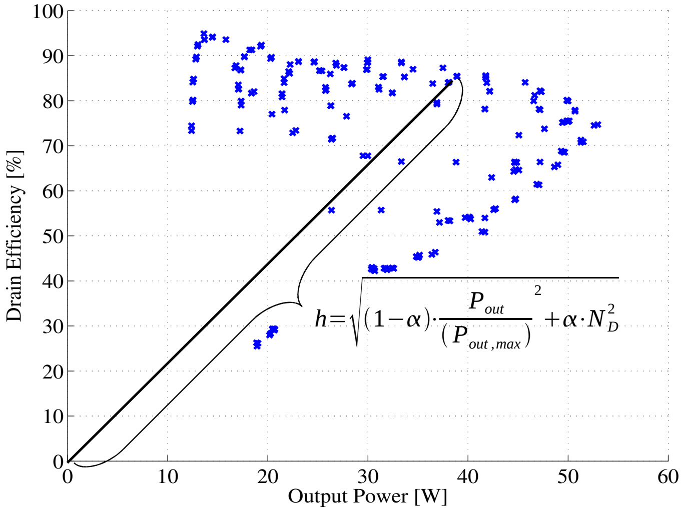


Fig. 4. Drain efficiency values for specific output power are plotted as obtained by the load pull measurement (Figure 3(a)). The distance of each point to the origin is used a as metric for optimization.

$$h = \sqrt{(1-\alpha)\cdot\left(\frac{P_{\mathrm{OUT}}}{P_{\mathrm{OUT,\,max}}}\right)^2 + \alpha\cdot\eta_D^2} \qquad (1)$$

- In the case when the output power is maximized without concern for efficiency, the parameter $\alpha = 0$.
- In the case when the efficiency is maximized without concern for output power sacrifice, the parameter $\alpha = 1$.
- Typically, however, there would be a tradeoff between this two parameters corresponding to different values of α between 0 and 1.
- When a parameter α is chosen for a given design the load pull data can be replotted to target the optimal impedance for a given tradeoff.

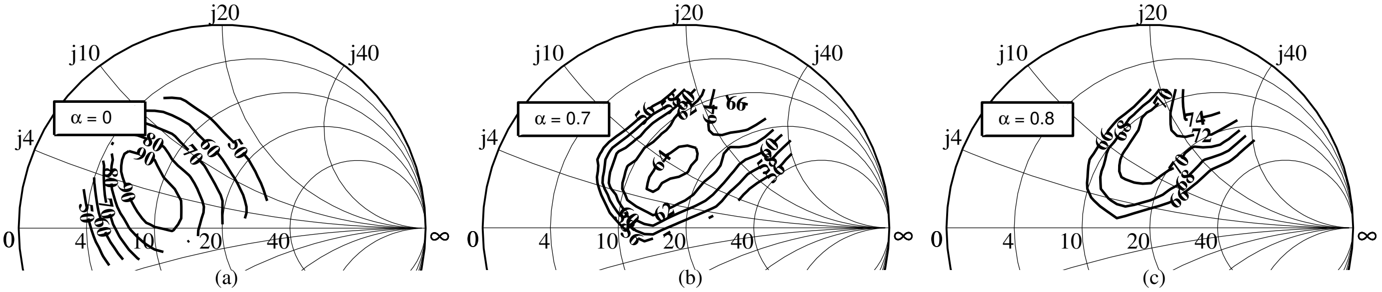
Examples are shown in Figure 5 for the load pull data corresponding to Figure 3(a). Load pull contours for different values of the parameter α in Equation 1 are chosen. High values of h mean that the specific requirements for a specific tradeoff are matched for all the impedances on this contour. For example $\alpha = 0.7$ (Figure 5(b) gives more weighting to efficiency than power. It seems that in this case the solution is not unique as there are two distinct contours that maximize the parameter h. This method can be extended to combine additional parameters in a slightly more complicated metric. For example, IMD level would be relevant for linearized Class-E PAs with envelope tracking [15]. In the presented design we choose $\alpha = 0.7$ and the resulting performance is presented in the next section.

TABLE I
MEASURED RESULTS FOR CLASS-E AMPLIFIER

V_{DS}	Pin	Pout	Gain (dB)	η_D	PAE
28 V	+32 dBm	45 W	14 dB	87%	84%
35 V	+33 dBm	65 W	15 dB	85%	82%
48 V	+34 dBm	87 W	15 dB	71%	70%

V. CLASS-E AMPLIFIER PERFORMANCE

A high–efficiency power amplifier was design and implemented for an impedance matching corresponding to $\alpha = 0.7$. The input and output matching impedances are $Z_{\mathrm{in}} = 10.1 + j1\,\Omega$ and $Z_{\mathrm{out}} = 12 + j6\,\Omega$. Input power sweeps were performed for the amplifier biased at 28 V, 35 V, and 48 V and the results are summarized in Table I. The amplifier achieves a maximum of 84% PAE with corresponding 87% η_{D} and 45 W of P_{OUT}. For a slightly higher supply voltage (35 V) the amplifier is able to deliver 65 W of P_{OUT} with little degradation in efficiency. For a supply voltage of 48 V the amplifier is able to deliver 87 W, with efficiencies close to 70%. Figure 1(b) shows the power sweep corresponding to a supply voltage of 28 V, while the cases corresponding to supply voltages of 35 V and 48 V are shown in Figure 6.



(a) (b) (c)

Fig. 5. Load pull contours in a normalized 20 Ω Smith Chart for different values of the parameter α in Equation 1. High values of h mean that the specific requirements for a specific tradeoff are matched for all the impedances on this contour; (a) show impedance contours for $\alpha = 0$, when power is optimize and efficiency is sacrificed, (b) $\alpha = 0.7$ gives more weighting to efficiency and (c) $\alpha = 0.8$ further maximizes efficiency.

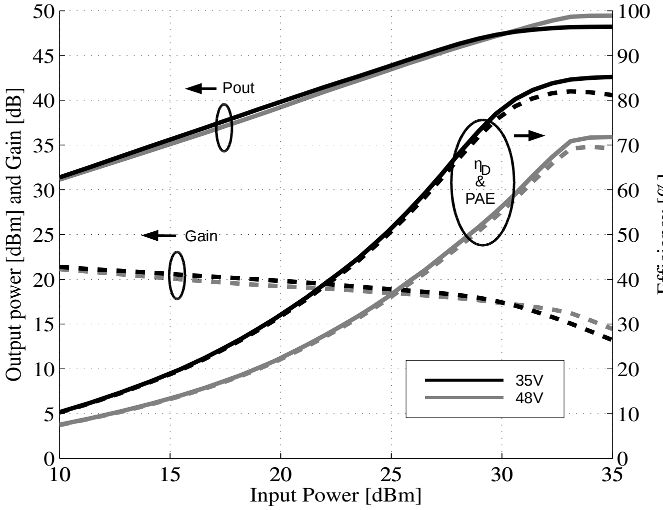


Fig. 6. Amplifier power sweeps for supply voltages of 35 V (black) and 48 V (gray) when the amplifier is operated at 370-MHz. The maximum PAE when the supply voltage is 35 V is 82 % with a drain efficiency of 85 % and an output power of 65 W. When the supply voltage is increased to 48 V the output power is 87 W, however the PAE drops to 70%.

VI. CONCLUSIONS

UHF PAs can benefit from wide–bandgap transistors due to their high power handling, high breakdown voltage, and low output capacitance. This work summarizes the design of a UHF high–efficiency power amplifier using a GaN HEMT on a SiC substrate transistor as the active device. The transistor was characterized with load pull techniques under class–E conditions. An optimization procedure based on a weighted Euclidean distance approach was used for impedance matching selection. This amplifier delivers 65 W of RF power at 370–MHz with 85% η_D and 82% PAE for a supply voltage of 35 V.

VII. ACKNOWLEDGEMENTS

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