Measuring Transistor Large-Signal Noise Figure for Low-Power and Low Phase-Noise Oscillator Design

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***Abstract*—This paper presents an experimental method for determining additive phase noise of an unmatched transistor in a stable 50-Ω environment. The measured single-sideband phase noise is used to determine the large-signal noise figure of the device. From the Leeson–Cutler formula and a known oscillator circuit with the characterized transistor, the phase noise of the oscillator can be predicted. The method is applied to characterization of several bipolar devices around 3.4 GHz, the frequency of interest for miniature rubidium-based atomic clock voltage-controlled oscillators.**

***Index Terms*—Large signal, noise figure (NF), oscillators, phase noise.**

I. Introduction

LOW PHASE noise is an increasingly important requirement for oscillator designers. In digital communications systems, close-in phase noise (or phase jitter in the time domain) affects the system bit error rate. In analog communications systems, close-in phase noise can limit channel bandwidth and broadband noise reduces the signal-to-noise ratio and the system sensitivity, especially after several repeater stations. In Doppler radar applications, the oscillator phase noise can set the minimum signal level that must be returned by a target in order to be detected.

The motivations of the work presented in this paper are miniature low-power high-quality atomic frequency standards and clocks [1]–[3]. The requirements for this new technology, often referred to as chip scale atomic clocks (CSACs), are pushing the state-of-the art in oscillator design in terms of simultaneous small size, low power consumption, and low phase noise. To effectively modulate the laser light field required for atom excitation, the local oscillator (LO) frequency must be equal to the hyperfine ground-state splitting frequency for Cesium atoms (around 9.2 GHz) or rubidium atoms (around 6.8 GHz). Another common method, which uses double-sideband modulation of the laser diode, requires the LO to be at half of the hyperfine transition frequency, i.e., 4.596 GHz for cesium and 3.417 GHz for rubidium. In addition, the LO needs to be tunable over approximately 2 MHz to compensate for frequency differences due to temperature, buffer gas pressure, and other variables [4]–[7].

One of the parameters that can aid in predicting the final oscillator phase noise is the transistor noise figure (NF) [8], [9], which is given in most manufacturers' data sheets, but is measured under small-signal conditions. In oscillators, transistors operate in large-signal mode, usually 2–3 dB in compression. In [10], it is experimentally shown that many amplifiers exhibit an increase in broadband noise of 1–5 dB as the input signal increases, and the NF in terms of single-sideband phase-modulation noise is given by

$$\mathrm{NF} = -N_{\mathrm{th}} + P_{\mathrm{in}} + L_a(f) \tag{1}$$

where N_{th} is the room-temperature single-sideband thermal noise and is equal to -177 dBm/Hz, P_{in} is the signal power in decibels (referenced to milliwatts) in a 1-Hz bandwidth and is assumed to be bandwidth independent, and $L_a(f)$ is the phase noise density in decibels (referenced to the carrier)/hertz. This is the wideband noise floor of an amplifier. Recently, a new study of PM noise and NF of low-noise amplifiers (LNAs) in a large-signal condition was discussed in [11] with the expected conclusion that saturated amplifiers have increased NF [12], [13].

Once all the variables are known, one can relate them and theoretically calculate oscillator phase noise using the following equation [14], [15]:

$$L(f_m) = L_a + 10\log_{10} \times \left[\left(1 + \frac{f_0^2}{(2 \cdot f_m \cdot Q_{\mathrm{loaded}})^2}\right) \cdot \left(1 + \frac{f_c}{f_m}\right)\right] \tag{2}$$

where

$L(f_m)$	ratio of the phase noise in a 1-Hz bandwidth to the sinusoidal source level expressed in decibels;
L_a	obtained from (1);
f_m	center frequency offset;
f_0	center frequency;
f_c	noise edge of the flicker or $1/f$ noise of the active oscillator;
Q_{loaded}	Q of the loaded resonator.

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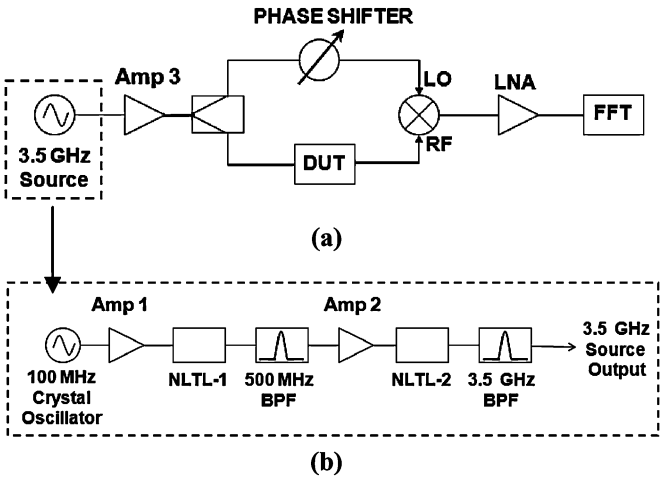

Fig. 1. (a) Block diagram of the additive phase noise measurement system. (b) Details of 3.5-GHz source. The signal from a 100-MHz oven-controlled crystal oscillator is multiplied using two NLTLs.

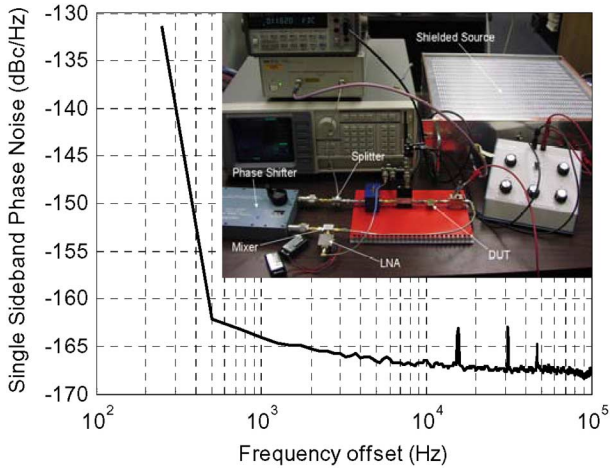

Fig. 2. Additive phase-noise system and its measured noise floor.

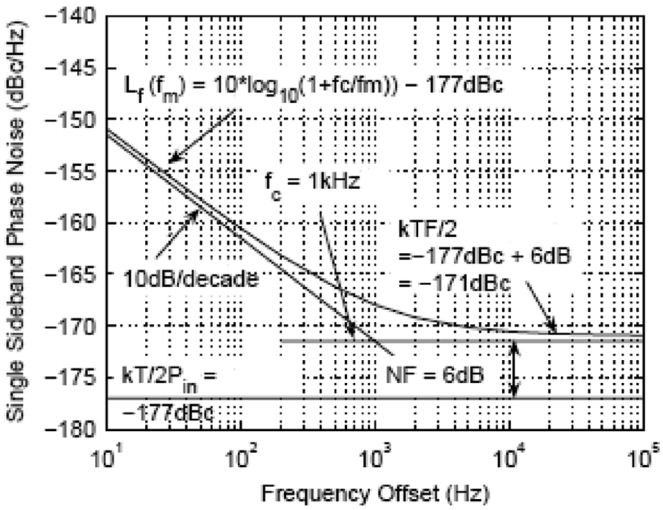

Fig. 3. Interpretation of noise measurements; e.g., assuming an input power to the amplifier $P_{\rm in}$ of 0 dBm, the noise floor will be -177 dBc/Hz. Transistor NF is 6 dB.

The goal of this paper is to present a new and relatively simple experimental technique for predicting oscillator phase noise with a given transistor by measuring the stable transistor additive phase noise as the bias varies.

II. Additive Phase-Noise Measurement

A system for large-signal NF measurements, which requires two identical devices-under-test (DUTs), was presented in [11]. The devices that were characterized for large-signal NF in [11] were 50-Ω prematched LNAs. In the measurement system presented here and shown in Fig. 1, both prematched and unmatched devices can be characterized, and there is no need for two identical DUTs. To ensure that the noise contribution of the measurement system is significantly lower than the phase noise of the transistor under test, a very clean source at 3.5 GHz is required. A 100-MHz oven-controlled crystal oscillator (Wenzel 501-04516D) is chosen as the fundamental source. Due to their high Q factors, lower frequency crystal oscillators multiplied several times (in this case, 35) typically exhibit better phase noise than available fundamental-frequency oscillators at S-band.

The 100-MHz output signal is amplified through an LNA (Hittite HMC479MP86) to a 50-mW level into a 50-Ω load. The output of the amplifier is connected directly to a nonlinear transmission line (NLTL), which operates as a low phase-noise comb generator or frequency multiplier and is described in more detail in Section II-A. The first NLTL, NLTL-1, generates significant harmonics up to 1 GHz, and the 500-MHz signal is filtered out. It is amplified using two cascaded amplifiers (Hittite HMC482ST89) with a total of 30-dB gain and 50-mW output power. The amplified 500-MHz signal is multiplied by a subsequent NLTL-2, which generates the required 3.5-GHz harmonic at around -15-dBm power level. The other generated harmonics are suppressed by at least 30 dB through a 3.5-GHz bandpass filter. The signal is amplified using a 35-dB gain HP 8449B preamplifier and is used as a 3.5-GHz source for the additive phase-noise measurement system shown in Fig. 1(b).

The additive phase-noise system is composed of a 3.5-GHz source explained earlier, a power splitter, a phase shifter, and a mixer [see Fig. 1(a)]. The phase shifter establishes true phase quadrature between the two signals at the mixer inputs, which provides cancellation of the main 3.5-GHz signal source. The output of the mixer after amplification is fed to a Stanford Research Systems SR760 FFT spectrum analyzer. The measured rms voltage spectral density corresponds to the additive phase noise of the DUT; in our case, a transistor. The system with the 3.5-GHz source provides a noise floor of -168 dBc/Hz at 100-kHz offset from the carrier (Fig. 2), which is much lower than the phase noise of the transistors under test.

Once the additive phase noise of a transistor $L_a(f)$ is measured, using (1) we can determine the large-signal NF of the device. Another advantage of this measurement is that it yields information about the flicker $(1/f)$ noise of the transistor in the amplifier circuit. This information is not provided in data sheets of active devices. Fig. 3 demonstrates how the noise measurements are interpreted. The lines show an example of how to calculate the NF from a given data set. Assuming an input

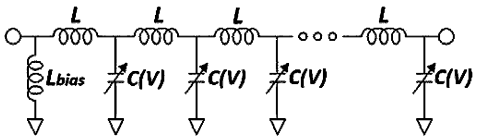

Fig. 4. Simplified NLTL schematic where the inductors are ideal lumped elements, and the varactors are represented by ideal variable capacitors.

power to the amplifier, $P_{\rm in} = 0$ dBm, the noise floor will be -177 dBm/Hz. The amplifier increases the noise floor by its NF of 6 dB in this case to -171 dBc/Hz. Close to the carrier, the flicker noise of the amplifier increases the phase noise at 10 dB/decade with a corner frequency $f_c = 1$ kHz.

A. NLTL Multipliers

The unique part of the measurement setup is the source, which includes two NLTLs. In [16], it is shown that appropriately biased NLTLs have excellent phase-noise performance as frequency multipliers, approaching the theoretical limit of

$$L(Nf) = 20\log N + L(f) \tag{3}$$

where N is the fundamental frequency multiplication factor. $L(Nf)$ in decibels is the phase noise at the Nth harmonic frequency and $L(f)$ in decibels is the phase noise at the fundamental at the same offset. The NLTLs from Fig. 1 are periodic artificial lumped-element transmission lines, as shown in Fig. 4. Typically, a varactor is used as a voltage-variable capacitor, resulting in a voltage-dependent phase velocity. With large-signal input voltage, the voltage variation of the NLTL capacitance results in nonlinear wave propagation and harmonics of the input frequency are generated. In nonlinear simulation, parasitics of inductors and a full SPICE model for varactor should be used [17]–[21].

The inductors in the eight-stage NLTL-1 are all equal with $L_1 = 10$ nH and the variable capacitors are hyper-abrupt varactor diodes with zero bias capacitance of 9 pF and the lowest capacitance of 0.6 pF at higher voltages. The characteristic impedance of the line is around 50 Ω for the midbias point. NLTL-2 is implemented similarly as an eight-section line with $L_2 = 4$ nH and a different diode with a capacitance range from 2 pF (zero bias) to 0.5 pF. The diodes are reverse biased. The multiplication efficiency for NLTLs is low: for 17 dBm of input power at 100 MHz, the 500-MHz output of NLTL-1 is approximately -11 dBm.

Alternative multipliers using, e.g., step recovery diodes (SRDs), have been shown to have an inferior phase noise. In [16], the phase noise of a Herotek GC200RC (SRD) comb generator is compared to a PicoSecond LPN7110 (NLTL) comb generator at the 200-MHz fundamental. For $P_{\rm in} = 24$ dBm, the measured phase noise for the SRD comb generator at a frequency offset of 10 kHz is -179 dBc/Hz, while the phase-noise measurement for the NLTL is -172 dBc/Hz at the same offset. The NLTL demonstrates near $20\log N$ multiplication behavior, while the SRDs is measured to have a 40-dB increase for $N = 10$ multiplication, or a $40\log N$ relationship [22].

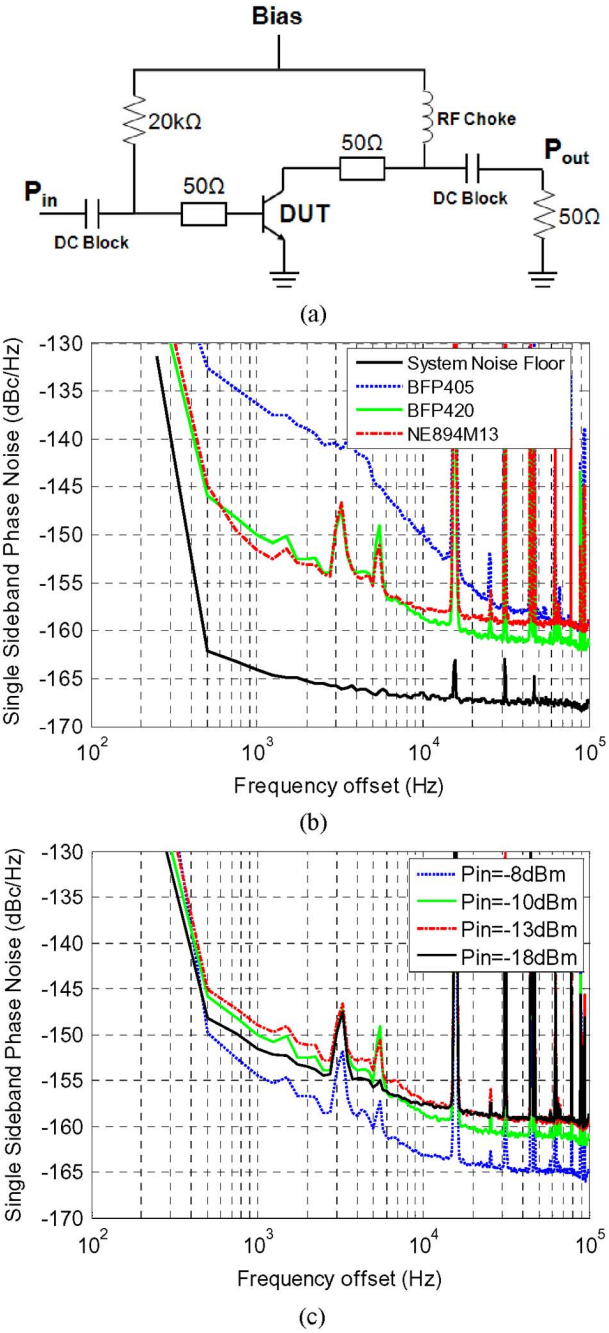

Fig. 5. (a) Testing circuit environment. (b) Additive phase-noise measurements of each transistor at $V_{\rm bias} = 2$ V and $P_{\rm in} = -10$ dBm. (c) Additive phase-noise measurements of the BFP420 device at $V_{\rm bias} = 2$ V and $I_{\rm bias} = 3$ mA for varying $P_{\rm in}$ over a 10-dB range.

III. Measurement Results

To demonstrate the method described above, the additive phase noise at 3.5 GHz was measured for the following three different bipolar junction transistor (BJT) transistors:

1) Infineon BFP405;
2) Infineon BFP420;
3) NE894M13 from California Eastern Labs (CEL).

The transistors are inserted in a 50-Ω environment without any matching circuits at input or output, and with emitters grounded and base bias resistors of 20 kΩ, as in Fig. 5(a). Fig. 5(b) shows the measured system noise floor and additive phase noise for all

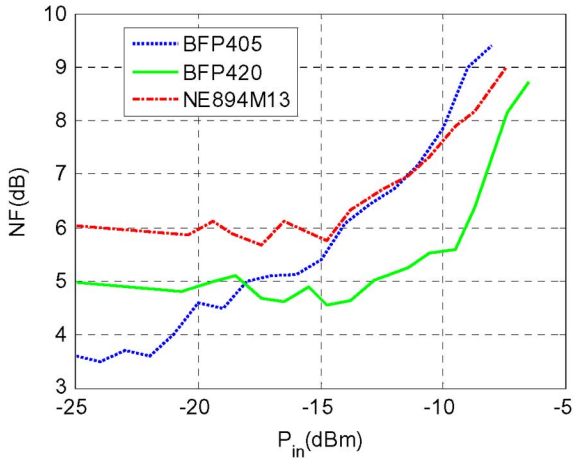

Fig. 6. Measured NF for different devices with different input power at $V_{\rm bias} = 2$ V. The small-signal NFs from the specification sheets are 1.25, 1.1, and 1.4 dB for the BPF405, BFP420, and NE894M13 devices, respectively.

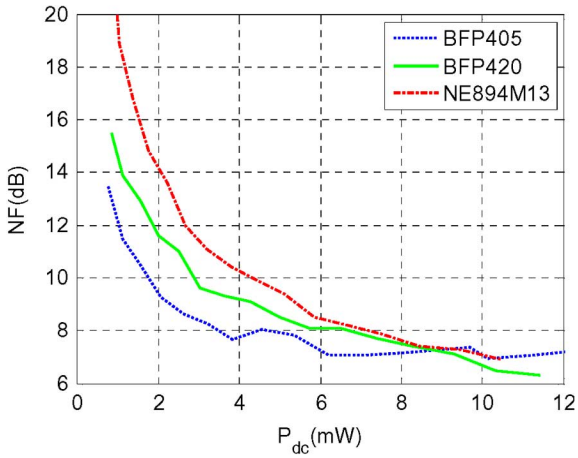

Fig. 7. Measured NF for three different devices. Transistors are driven 3 dB into saturation in each case.

three transistors at $V_{\rm bias} = 2$ V and $P_{\rm in} = -10$ dBm. The last data point, at 100-kHz offset, is considered the thermal noise level and the NF of the transistor is calculated from (1) [7]. The measured phase noise for the given conditions from Fig. 5(b) shows that the BFP405 Si bipolar has the worst NF for low-frequency offsets. The NF is 15 dB higher at 1 kHz compared to the other two devices, and 30 dB above the noise floor. The spikes in the measurements are due to interference from the screen in the fast Fourier transform (FFT) spectrum analyzer instrument. One can also notice that the flicker corner for BFP420 and NE894M13 is around 10 kHz, while it is much higher for the BFP405 transistor. Fig. 5(c) shows the additive phase-noise measurements of a single transistor (BFP420) obtained at different input signal levels ($P_{\rm in}$) and constant $V_{\rm bias} = 2$ V.

Fig. 6 illustrates the large-signal NF of the transistors and its dependence on the input power up to around 4-dB gain compression. The transistors are at $V_{\rm bias} = 2$ V. There is an increase in NF compared to the small-signal value given in the data sheets. This effect is due to the nonlinearity in the transistor manifested as AM to PM conversion.

Fig. 7 illustrates the large-signal NF measurements at different bias points. The input power level presented to the transistors is around -11 dBm for BFP405 and around -8 dBm for BFP420 and NE894M13. At these power levels, the transistors are at 3-dB saturation points. As expected, the NF decreases as the voltage is increased.

The plots in Figs. 5–7 are chosen to illustrate the importance of characterization at different power levels and bias points. For example, Fig. 6 indicates that the BFP405 device (dotted line in this figure) seems to have the largest phase noise, but if dc power consumption is an important parameter, Fig. 7 indicates that the BFP405 device is the optimal choice for oscillator design since it has the lowest large signal NF for low dc power levels.

IV. Discussion and Design Example

Cutler and Leeson derived an equation describing the observed phase noise of an oscillator as a function of circuit component properties [8], [9]. Based on this work, the derivation of (2) is detailed in [14] and [15]. As an example, a VCO around 3.4 GHz is designed using the BFP405 transistor

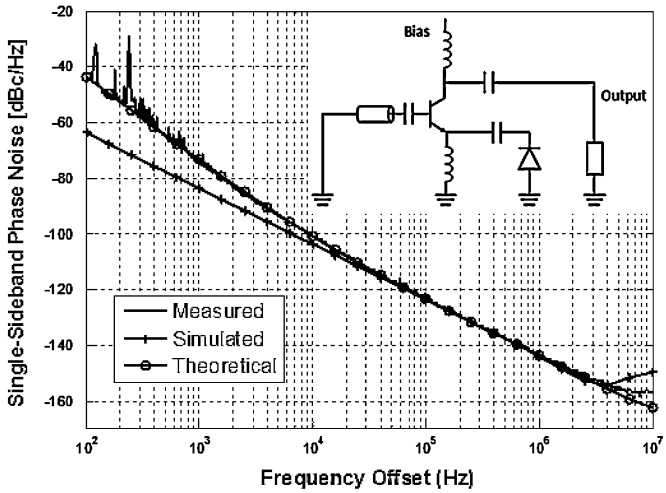

Fig. 8. Measured, simulated, and calculated phase noise for the 3.4-GHz oscillator for the oscillator circuit shown in the inset and described in the text.

based on the measurements in Figs. 5–7. The oscillator circuit topology is shown in Fig. 8 in the inset and details are presented in [23]. Using the experimental data discussed here and (2), the 3.4-GHz oscillator phase noise is computed and compared to the measured and simulated phase noise for $V_{\rm bias} = 3$ V ($P_{\rm dc} = 7$ mW), as shown in Fig. 8.

The phase noise of the oscillator was measured to a 100-kHz offset directly using the discriminator method [24] with a 125-ns low-loss coaxial delay line. This measurement was verified by evaluating a commercial dielectric resonator oscillator (DRO) and comparing to the DRO characteristics obtained using an Agilent E5500 phase-noise measurement system. The technique enables phase noise measurements down to -115 dBc/Hz at 10-kHz offset at fundamental frequencies of up to 10 GHz, 13 dB below our measurement. For this measurement, the output signal from the oscillator is amplified to approximately 17 dBm. Half of this power is sent to the LO port of a low-noise mixer and the other half through a delay line and phase shifter. This signal is mixed in quadrature at the RF port of the mixer and the IF output is amplified and measured by a Stanford Research Systems SR760 FFT spectrum analyzer.

The oscillator performance is simulated using Agilent's Advanced Design System (ADS) software. Note that there is a

slight discrepancy between the simulated and measured phase noise at frequencies close to the carrier in Fig. 8. This is attributed to the device model not including flicker noise, resulting in steady 20-dB/decade prediction, even close to the carrier.

In summary, the acceptable agreement between the three curves in Fig. 8 shows that the experimental method for determining large-signal transistor NF presented in this paper is useful for choosing the active device for oscillator design. This method was applied to other bias points and similar results were obtained. The method enables the optimal choice of transistor when phase noise, dc power consumption, and output power are considered simultaneously.

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