

Design Method for UHF Class-E Power Amplifiers

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Abstract— This paper describes a method for designing single-ended high-efficiency switched-mode class-E UHF power amplifiers. The design procedure consists of a modified load pull transistor characterization from which a power/efficiency metric is calculated. Results for four prototypes using different device technologies are presented in detail. Amplifiers with Si-LDMOS, SiC-MESFET, GaN-HEMT on a Si substrate, and GaN-HEMT on a SiC substrate produce power over 40W with power-added efficiency greater than 75% and gain between 13 dB and 17 dB.

Index Terms— UHF power amplifiers, Switching amplifiers

I. INTRODUCTION

In a high-power UHF or microwave transmitter the final stage power amplifier (PA) dominates the loss budget. Efficiency of this stage can be improved by operating it at or beyond the 1-dB compression point at the expense of linearity. Harmonic control offers an additional increase in efficiency when the device has sufficient gain at harmonics of the center frequency. The class-E mode of operation takes advantage of deep compression, low-quiescent current bias point, and harmonic control to achieve ultra-high efficiency. Linearity can be achieved using external circuits (e.g. EER, LINC [1]).

Class-E PAs have been shown to achieve 95% drain efficiency in the low-MHz range [2], 84% at UHF [3], [4], 75% at 2 GHz [5], and 70% at X-band [6]. In this mode the transistor is assumed to operate as an ideal switch and therefore must have an f_T significantly higher than the frequency of operation. Recent progress in wide band gap semiconductor technology [7], [8], [9] has significantly extended the frequency range of large periphery devices, making the class-E approximation reasonable for high-power transistors.

Nonlinear models which adequately model device operation in the low-quiescent current regime are not readily available for these devices, and load pull becomes a standard approach for obtaining empirically based device models. However, standard load pull measurement techniques do not provide the data required for class-E design. Here we demonstrate a modified load pull method applied to four transistor technologies: (1) a Si-LDMOS from Triquint (AGR09045E); (2) a SiC-MESFET from Cree (CRF24060); (3) a GaN HEMT on a Si substrate from Nitronex (NPTB00050); and (4) a GaN-HEMT on a SiC substrate from RFMD (RF3932). The paper organized as follows:

- Section 2 describes the class-E mode of operation and design procedure, including a modified load pull technique.
- Section 3 includes device and load pull characterization data for each transistor using a break-apart fixture as shown in Figure 1.
- Section 4 details design and performance of class-E PA prototypes at 370 MHz based on the four devices.

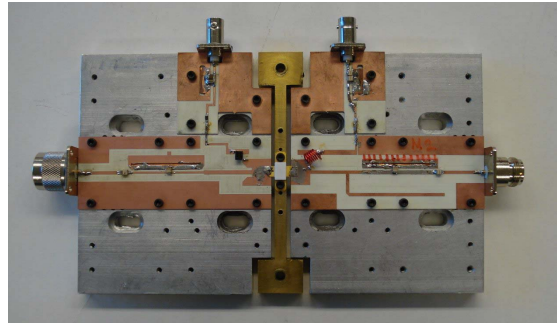


Fig. 1. Photograph of the break-apart fixture used for pre-matched harmonic-tuned load pull characterization. The second harmonic open load circuit is realized with an open stub. Bias networks are included. The active device can be replaced with TRL standards during load pull calibration.

II. CLASS-E PA DESIGN METHODOLOGY

High efficiency is obtained in the class-E mode by minimizing overlap of the current and voltage across the device output. There are three conditions which must be satisfied in the time domain [e.g. [10]]:

- $i_D = 0$ when the switch stops conducting;
- $v_{DS} = 0$ when the switch begins conducting;
- $dv_{DS}/dt = 0$ when the switch begins conducting;

These conditions are satisfied for a 50% duty cycle when the fundamental impedance is

$$Z_E = \frac{0.28}{\omega_s \cdot C_{OUT}} e^{j49^\circ} \quad (1)$$

where C_{OUT} is the parallel combination of C_{DS} with ($C_{GS} + C_{GD}$) and ω_s is the switching rate in radians [11]. Additionally, all harmonics are presented with an open circuit at the output. Note that the ideal load impedance is a function only of frequency and the device output capacitance, which can be estimated from S-parameters.

High power transistors typically require very low load impedances due to a large number of parallel unit cells. Pre-matching networks internal to the package are often included in commercial devices in order to facilitate matching over a broad band. This introduces another impedance transformation inside the package which makes class-E matching at the fundamental and harmonic more complicated. For this reason we limit device selection to those without internal output pre-matching. A good initial approximation of input impedance is a conjugate match, also obtained from device S-parameters.

Non-sinusoidal voltage and current waveforms result when the class-E conditions listed above are satisfied. These waveforms are rich in harmonic content and have voltage and current maximum swings given by

$$V_{DS,max} = 3.56V_{DS} \quad I_{DS,max} = 2.86I_{DS} \quad (2)$$

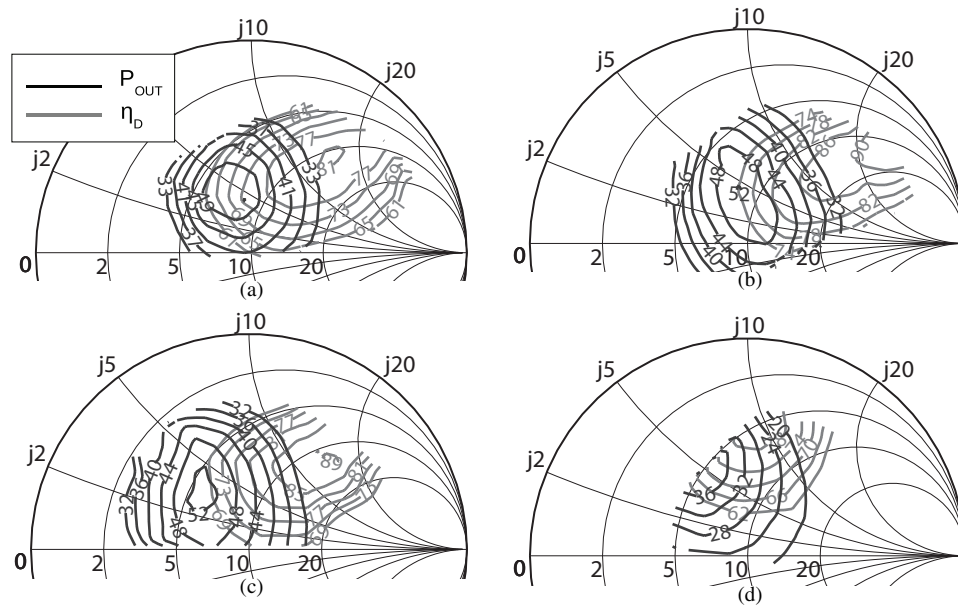


Fig. 2. P_{OUT} and η_D load-pull contours in a $10\text{-}\Omega$ Smith Chart for each of the four different transistor technologies at a supply voltage of 28 V. (a) GaN HEMT on a Si substrate, (b) GaN HEMT on a SiC substrate, (c) SiC MESFET, and (d) Si LDMOS. Notice that optimum P_{OUT} contours do not overlap with optimum η_D contours.

C_{OUT} is dominated by C_{DS} , and very large periphery devices with many parallel cells have large nonlinear intrinsic drain capacitance. As a result of this nonlinearity the peak of the drain current waveform can be significantly higher (e.g. up to 30% for a square root nonlinearity [12]). These increased peak drain voltage and current values stress the device and must be taken into account when selecting bias conditions.

The theoretical class-E mode is capable of 100% drain efficiency but in reality is limited by intrinsic resistances inside the transistor, losses in input, output, and bias circuits, and parasitic reactance leading to drain voltage and current overlap. Important parameters when choosing a device for class-E operation therefore include C_{OUT} , packaging, f_T , breakdown voltage, maximum current, R_{ON} , and in addition maximum junction temperature as summarized in Table I.

Typical load pull uses mechanical tuners to present a constellations of impedances to the transistor source and load, yielding an empirical device model. For low impedance high-power devices, optimal device impedances are not close to the standard $50\text{-}\Omega$. Therefore, load pre-matching circuits are used to transform the tuner's $50\text{-}\Omega$ constellation to one centered at the ideal class-E impedance of Equation 1. The source pre-matching circuit is similarly transformed to the conjugate match determined using S-parameters. To achieve accurate load pull results, careful calibration of the fixture and all other

parts of the system is required. A modular fixture is designed in which input circuit, output circuit, and device are separate blocks. The ability to remove the device under test and insert standards allows TRL calibration, removing the effects of bias and pre-matching circuits.

In addition to transforming the fundamental impedance the pre-matching circuit also needs to transform all harmonic impedances to an open, per the class-E requirement. In practice only the second harmonic is considered because it has the largest effect. This termination is achieved using a quarter-wave open-circuit stub placed a quarter wave from the device as shown in Figure 1. Finally, the load pull test fixture includes bias circuits placed close to the device to increase low-frequency stability.

III. TRANSISTOR CHARACTERIZATION

Figure 2 shows load pull data for each of the transistors at 370 MHz when biased with a drain supply voltage of 28 V and quiescent current just above cutoff (approximately 10 mA). The source impedance for each of these measurements is chosen to obtain maximal gain. It is interesting to observe how the contours depend on C_{OUT} and device periphery, e.g. the optimal impedances for Si-LDMOS are smaller compared to the other transistor technologies due to the significantly larger device periphery and output capacitance.

TABLE I
SUMMARY OF TRANSISTOR PROPERTIES AND RESULTS OF CLASS-E LOAD PULL CHARACTERIZATION

Device	V_{DSS}	C_{OUT}	R_{ON-DC}	T_j	V_{TH}	Optimum P_{OUT}	Optimum η_D
16-mm GaN/Si HEMT	100 V	9 pF	0.23 Ω	200°C	-2.1 V	63 W, 68% @ $5+j7.5\Omega$	30 W, 84% @ $14+j22\Omega$
10-mm GaN/SiC HEMT	150 V	9 pF	0.32 Ω	250°C	-4.2 V	53 W, 75% @ $8+j4.4\Omega$	14 W, 93% @ $11.8+j2.9\Omega$
30-mm SiC-MESFET	120 V	11 pF	0.46 Ω	250°C	-10 V	53 W, 70% @ $6+j3.6\Omega$	20 W, 89% @ $13.5+j16\Omega$
120-mm Si-LDMOS	65 V	23 pF	0.35 Ω	200°C	3.5 V	40 W, 74% @ $5.2+j5.6\Omega$	24 W, 82% @ $4+j9.3\Omega$

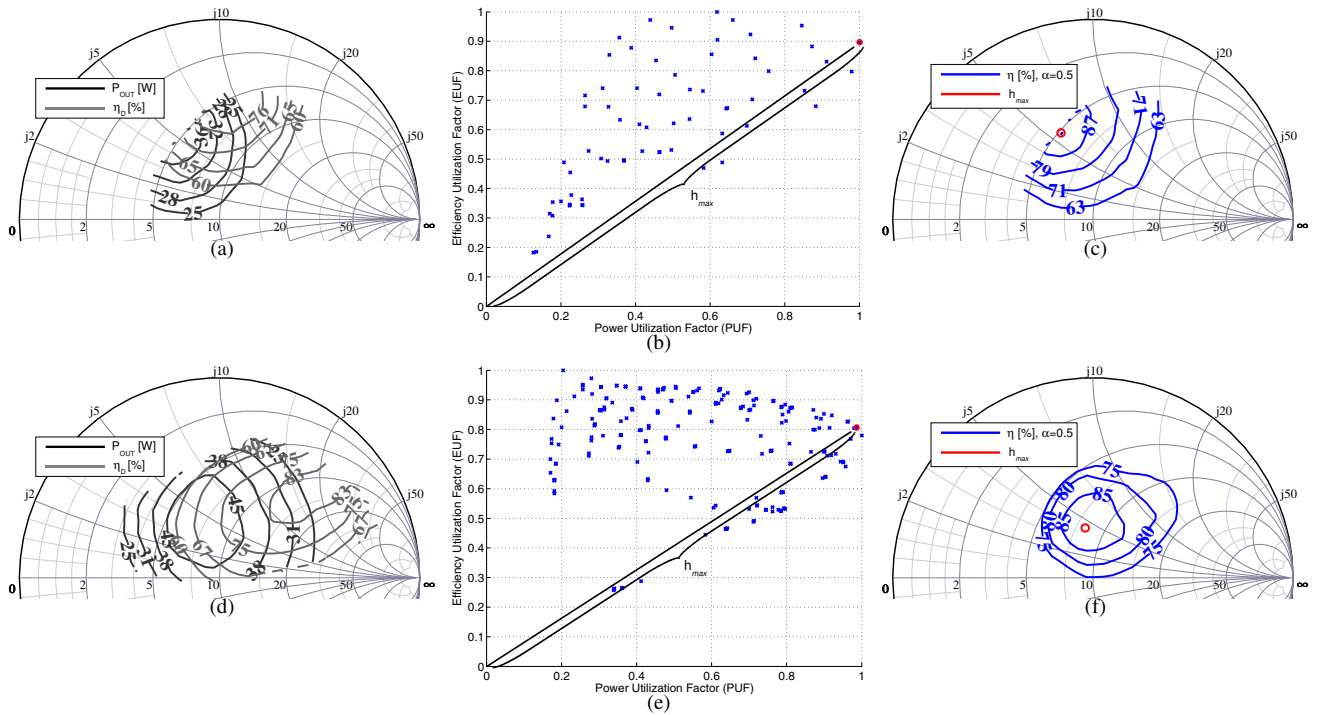


Fig. 3. (a) and (d) show load pull data for the Si-LDMOS and the GaN on Si devices with contours of output power and drain efficiency. For each impedance on the contours the normalized efficiency (EUF) is plotted vs. normalized power (PUF) in (b) and (e). For a weighting factor $\alpha = 0.5$ and based upon Equation (1) the metric h is plotted on the smith charts of (c) and (f).

These contours vary significantly from traditional load pull results obtained without explicit harmonic terminations. Notice that the degree to which regions of high output power and high efficiency overlap varies among the different technologies, and a tradeoff exists between optimum-power and optimum-efficiency designs. The results are summarized in Table I.

For a particular PA design it would be useful to have a guideline to determine the tradeoff between output power and efficiency. For each impedance of the measured load pull data in Figures 3(a) and 3(d), the measured output power is normalized and plotted versus normalized efficiency in Figures 3(b) and 3(e). A metric h is defined as a weighted Euclidean distance of each point from the origin

$$h = \sqrt{(1 - \alpha) \cdot \left(\frac{P_{OUT}}{P_{OUT, max}} \right)^2 + \alpha \cdot \left(\frac{\eta_D}{\eta_{D, max}} \right)^2} \quad (3)$$

This metric is then plotted on Figures 3(c) and 3(f) for a given weighting factor α for two of the devices. For example, when the output power is maximized at the expense of efficiency $\alpha = 0$. For equal weighting of both parameters $\alpha = 0.5$ and is plotted in Figure 3 for the Si-LDMOS and the GaN on Si devices.

IV. PA PROTOTYPES

Four PA prototypes were designed to achieve a minimum of 40 W output power, with the resulting weighting factors (α) in Table II. The value of α in this case is an indicator of how much power or efficiency could be improved for a given device by adjusting the matching.

TABLE II
PROTOTYPE PA POWER SWEEP PERFORMANCE

Part Number	V_{DS}	α	P_{OUT}	Gain	η_D	PAE
GaN/Si HEMT	28 V	0.5	43 W	17 dB	83%	81%
GaN/SiC HEMT	28 V	0.5	45 W	15 dB	85%	82%
SiC-MESFET	35 V	0.7	41 W	15 dB	80%	78%
Si-LDMOS	18 V	0.5	43 W	13 dB	80%	75%

The load pull data presented in the previous section was collected with a second harmonic termination which must be included in PA prototype designs. Measured performance at 370 MHz of the four PA prototypes is shown in figure 4 (a) and (b). Gain and PAE were measured as a function of output power with constant drain voltage. This voltage varies per prototype to prevent drain voltage breakdown as previously discussed in Equation 2. The optimal gain for each of the 370-MHz amplifiers ranged between 18 dB and 22 dB and the compressed output power is above +46 dBm for all the amplifiers. Note that heavy gain compression is required to satisfy the switching approximation and achieve high-efficiency class-E operation. This implies highly nonlinear behavior, which can be corrected with the use of supply or load modulation techniques such as EER [13] and LINC [1].

Figure 4 (c) and (d) show output power and output voltage to a 50- Ω load as a function of supply voltage. In these type of measurement the input power is fixed to a constant value. Increasing the supply voltage, effectively increases the gain of the amplifier and the output power. The slope of the V_{OUT} lines depends on impedance selection. From this figure we can conclude that the Si-LDMOS matching gives more weight

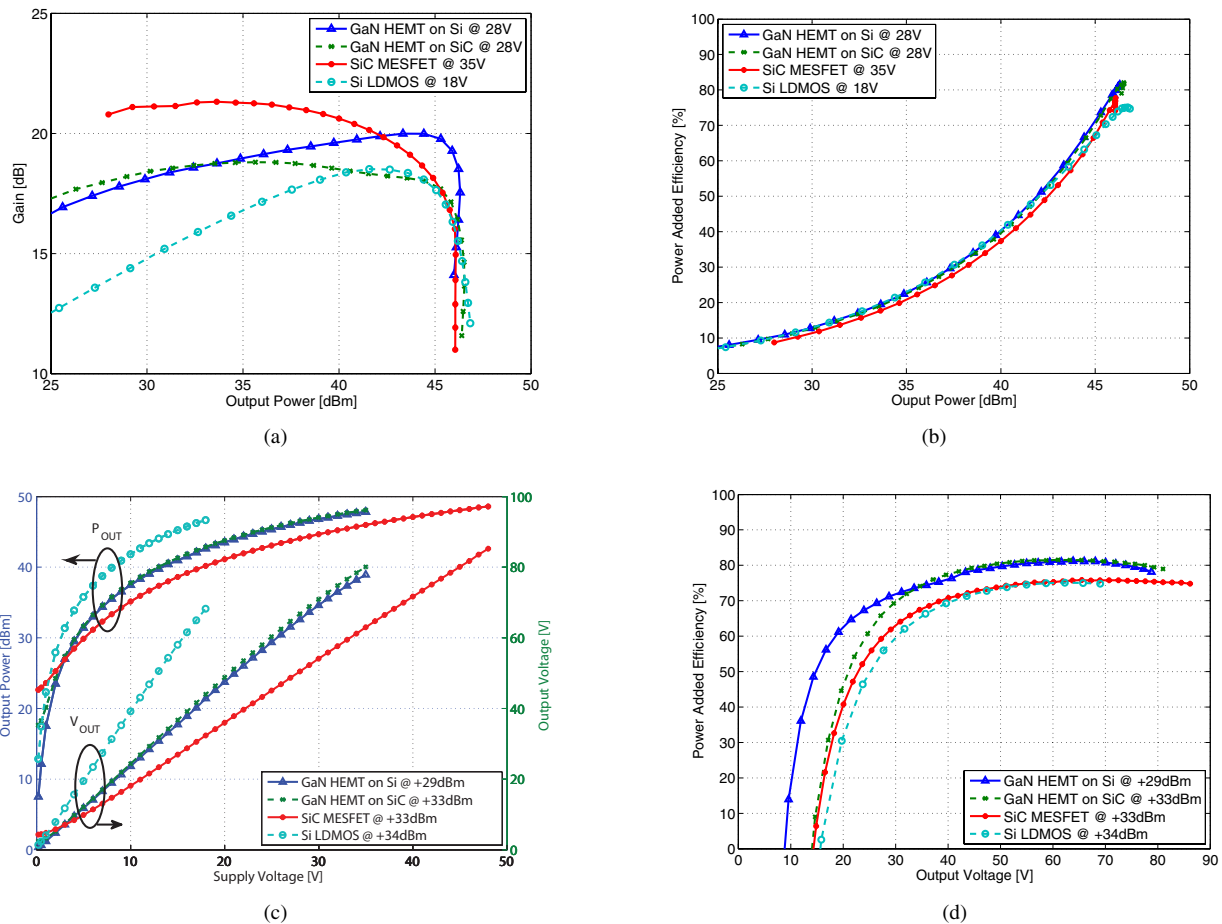


Fig. 4. Measured performance at 370 MHz of the four PA prototypes. (a) and (b) gain and PAE as a function of output power with the constant drain voltage noted in the legend. (c) output power and voltage across a $50\ \Omega$ load as a function of drain supply voltage for a fixed input power, noted in the legend. (d) PAE as a function of output voltage for a fixed input power.

towards achieving maximal output power at a lower voltage compared to the other technologies, so it has a larger slope. Figure 4(d) shows PAE vs. V_{OUT} for each of the amplifiers showing that output voltage variations can be achieved while maintaining an overall high PAE.

V. ACKNOWLEDGEMENTS

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