

Planar Circuits for Non-contact Near-Field Microwave Probing

Jonathan D. Chisum¹, Mabel Ramírez-Vélez, Zoya Popović

Department of Electrical and Computer Engineering, University of Colorado at Boulder
Boulder, CO 80309, USA

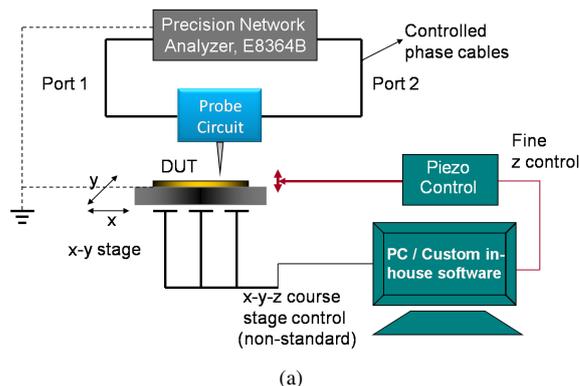
¹chisum@colorado.edu

Abstract—This paper presents a planar microwave probe circuit for non-contact near-field probing of quasi-planar structures which can be made of metal, dielectric or semiconductor. The probe circuit demonstrated here consists of a high-Q resonator in the range between 900 MHz and 5 GHz hybridly integrated with a microstrip circuit and field-concentrating micro-meter size probe tip which determines the spatial resolution of the detection process. The design of the probe circuit and measurement system are presented, along with measurements of a GaAs test circuit and a Si CMOS chip. By scanning the probe above a quasi-planar sample, two-dimensional data sets of complex S-parameters are obtained and appropriate processing is applied to extract information about the sample.

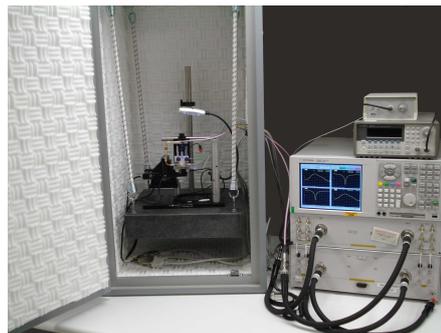
I. INTRODUCTION

Near-field microwave probing has been used in the past few decades for material property measurements by loading a resonant circuit with the unknown material, usually in the form of a planar slab [1],[2]. This non-contact method does not require placing the sample in a large, high quality factor (Q) cavity. For example, a probe based on a coaxial ($n\lambda/2$) line with tapered electrodes showed the possibility of measuring semiconductor resistivities between 0.5 and $100 \Omega \cdot \text{cm}$ as early as 1965 [3]. A coaxial $\lambda/4$ cavity with a sharpened tip attached to the center conductor and with $Q \approx 730$ was used for spatially imaging the complex dielectric permittivity of various ceramic samples, enabling studies of structural defects, porosity, etc. [4]. A cavity resonator with a capacitive metal tip and $Q = 1700$ was demonstrated in [5] for characterizing complex dielectric constants of thin films at 1 GHz with a sensitivity of $\delta\epsilon/\epsilon = 10^{-5}$. Most of the probes are capacitive and large, roughly $2 \text{ cm} \times 2 \text{ cm} \times 10 \text{ cm}$. In [6],[7], compact dipole and loop (magnetic) probes implemented in low-Q 900 MHz microstrip were used for metal conductivity measurements, and to detect large sub-surface features on a PCB.

In this paper, the goal is to dramatically reduce the size of the resonant probe circuit while preserving the main performance metrics, such as high quality factor and detection of very small features. The experimental setup and the basic principle of operation is discussed along with probe circuit design and basic calibration. Measurement results are given for a GaAs multi-layer test circuit and Si CMOS chips.



(a)



(b)

Fig. 1. Block diagram (a), and photograph (b) of the near-field microwave probing setup. The motion stages, sample platform, and probing circuit are fixed in an acoustic vibration-isolation chamber. The PNA is connected to the probing circuit through phase stable, low-loss cables. In (b), the motion stages, and probe circuit are on the vibration isolation platform.

II. NEAR-FIELD MEASUREMENT SETUP

A block diagram of the near-field non-contact measurement setup is shown in Fig. 1(a). The probe circuit with the sharp field concentrating tip is mounted above the sample, which sits horizontally on a stack of Physik Instrumente (PI) M-11X series micro-translation stages. The micro-translation stages provide coarse xyz motion control while a PI P-611.ZS piezoelectric stage provides fine- z control. The two ports of the probe circuit are connected through low-loss, phase-stable cables to an Agilent E8364B Precision Network Analyzer (PNA). The coarse xyz motion stages are controlled through a PI C-843 motor driver controller card. The fine- z piezoelectric motion stage is controlled via a bias voltage from a function

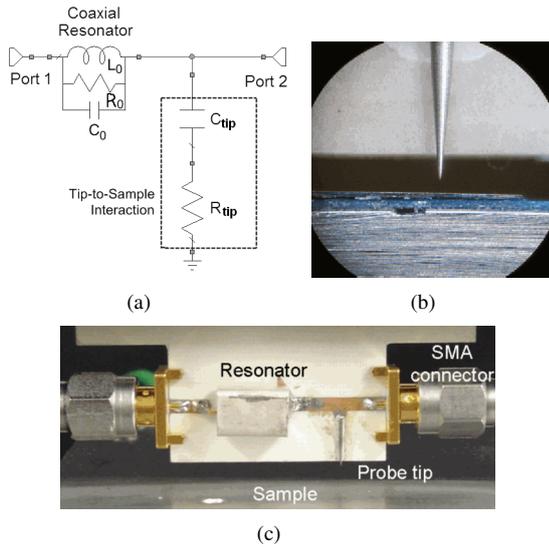


Fig. 2. (a) Simple equivalent circuit model of the probe above a sample, as shown in the photograph taken through the microscope (b). The probe circuit is shown in (c).

generator and a low noise amplifier. A computer triggers and records the four complex S-parameters measured by the PNA. Figure 1(b) shows a photograph of the setup. The Agilent N9445A passive acoustic vibration isolation chamber acts as a mechanical low-pass filter with a cutoff of approximately 2 Hz.

The principle of operation is based on loading a high-Q resonant circuit with the tip-to-sample impedance. A simple equivalent circuit of the probe above the sample is shown in Fig. 2(a). The resistance (R_{tip}) changes the loaded Q of the resonator, while the coupling capacitance (C_{tip}) changes the resonant frequency (f_0). L_0 , C_0 , and R_0 are equivalent lumped elements used to model the resonator. Figure 2(b) shows a micrograph of a $15\mu\text{m}$ tip above a sample, and Fig. 2(c) shows a photograph of the microwave probe circuit operating at 1.8 GHz. Because the response of the probe circuit is dominated by the resonator, perturbation theory can be applied to model the loading by the sample [8]. Expressions for the change in resonant frequency (Δf_0) and quality factor (ΔQ) can be derived in terms of a complex load capacitance, $C = C_{re} + jC_{im}$, as follows [5],[9]:

$$\frac{\Delta f_0}{f_0} = -\frac{C_{re}}{2C_0}$$

and

$$\Delta\left(\frac{1}{Q}\right) = \frac{1}{Q} - \frac{1}{Q_0} = -\left(\frac{1}{Q_0} + \frac{2C_{im}}{C_{re}}\right) \frac{\Delta f}{f_0}$$

where, $C_{re} = \frac{C_{tip}}{1+(\frac{\omega}{\omega_1})^2}$, $C_{im} = \frac{-\omega C_{tip}}{1+(\frac{\omega}{\omega_1})^2}$, and $\omega_1 = \frac{1}{R_{tip}C_{tip}}$.

III. PROBE CIRCUIT DESIGN

In the simple model of Fig. 2(a), the probe tip impedance models coupling of the probe tip to the surface of the sample, and the penetration of the fields into the sample. For samples

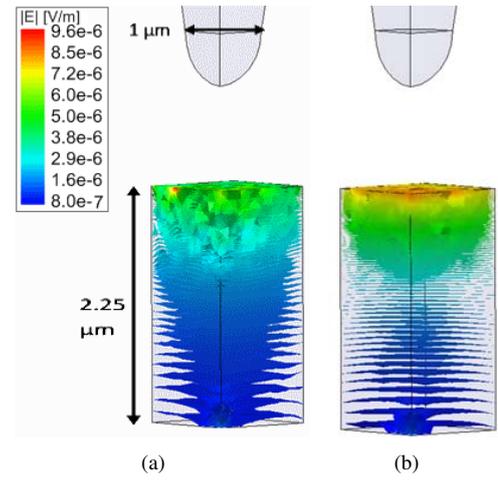


Fig. 3. Electric field magnitude in a $2.5\mu\text{m}$ thick aluminum slab with a $1\mu\text{m}$ probe excitation. The concentration of the electric field is shown at (a) 1 GHz and (b) 4 GHz.

with finite conductivity the penetration depth is larger at lower frequencies. In this work, probe tips with diameters of a few microns are used. To concentrate the field the probe tip is positioned on the order of one diameter above the substrate. For penetration depths on the same order of the probe tip, in conductive material, this implies using frequencies in the range from 0.5 to 5 GHz. This in turn, implies a very large probe circuit for a high-Q resonator. For example, a 10 cm long $\lambda/4$ coaxial resonator was used at 950 MHz in [10]. In contrast, the resonator in Fig. 2(c) is $6\times 6\times 8.5\text{ mm}$, (less than 1% of the volume), and operates at 1.8 GHz. This coaxial, $\lambda/2$ open-circuit resonator is filled with a high dielectric constant ($\epsilon_r \approx 90$) and exhibits a measured loaded $Q \approx 650$. The resonator is mounted in a microstrip circuit on Rogers 4003c substrate. The tips are tungsten probes, widely available in various tip diameters ranging from $1\mu\text{m}$ to $15\mu\text{m}$. Because the field from the tip is not a single frequency plane wave, the skin depth formula for penetration at the operating frequency cannot be applied. FEM simulations were performed for a $1\mu\text{m}$ diameter tip above a thick aluminum slab as shown in Fig. 3. Frequency components generated at the tip will penetrate different depths into the sample, and it can be seen that a probe operating at 1 GHz has further penetration depth than one operating at 4 GHz.

The ground plane of the microstrip circuit adds unwanted capacitance in parallel to the probe capacitance; therefore, in the probe design, an important factor is the extension of the tip beyond the ground plane. Figure 4 shows the equivalent capacitance, backed out from S-parameter measurements as the probe is moved away from an aluminum slab. The capacitance decreases dramatically up to $1\mu\text{m}$, as expected. However, after $1\mu\text{m}$ the capacitance begins to saturate due to the parasitic capacitance of the circuit which does not change as a function of height above a conducting plane. There is good agreement between the backed out capacitance from measurement, and the theoretical values for a simple parallel plate capacitance in

shunt with a parasitic saturation capacitance, as shown by the dashed line. It was found, through full wave HFSS simulations, that reducing the microstrip stub length and corresponding ground plane by 2 mm, reduces the parasitic capacitance of the circuit by 37%. This increases the percentage of total capacitance due to the tip-to-sample interaction from 4% to 23%, which increases overall sensitivity.

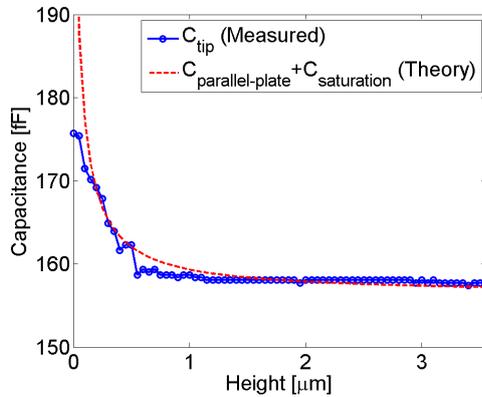


Fig. 4. Capacitance measured as a function of height above an aluminum slab. The dashed line shows the first order $1/z$ dependence plus a parasitic “saturation” capacitance before the circuit was redesigned to reduce the parasitic capacitance.

IV. MEASUREMENT RESULTS

Several test samples were characterized with probes designed to be resonant at 4.4 GHz, and 1.8 GHz. The first sample is a GaAs test structure fabricated in the TriQuint TQPED process as shown in 5(b). Four metal layers, Metal 0 ($0.4 \mu\text{m}$ of TiPtAu), a metal-insulator-metal (MIM) layer ($0.4 \mu\text{m}$ of Au), Metal 1 ($2 \mu\text{m}$ Au), and Metal 2 ($4 \mu\text{m}$ Au), separated by an insulator with a dielectric constant of 2.8, were used to create the offset and overlapping test structure as shown in Fig. 5(a). The probe was scanned at a height of approximately $20 \mu\text{m}$, with a step size of $20 \mu\text{m}$ in x and y . Figure 5(c) is the resulting resonant frequency measurement calculated from the zero-phase crossing of S_{12} . The resonant frequency changes by 350 kHz across the test structure. It is seen that the resonant frequency exhibits stepped features, corresponding to the 3D physical geometry of the test structure.

The second test structure is a large CMOS chip fabricated in a standard IBM process, consisting of four $400 \mu\text{m}$ squares of dense circuitry with eight metal layers. Two of the squares are shown in Fig. 6. The two square regions are not identical on the inner metal layers. In addition, the top two metal layers contain periodic metal polygons roughly $6 \mu\text{m}$ and $1 \mu\text{m}$ square, used for planarization. These metal squares provide an extra shielding layer for the demonstration of metallic depth penetration. A backside infra-red image (Fig. 6) shows the difference between the two circuits in Metal layer 4 clearly, whereas a top-side visible light microscope image would not show it.

The normalized Q-factor for the 2D scans obtained with a $15 \mu\text{m}$ diameter tip, $5 \mu\text{m}$ above the sample surface, at

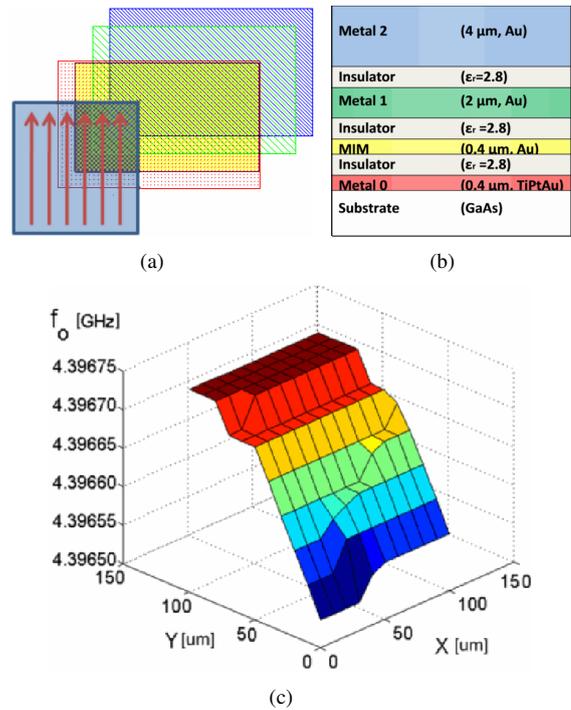


Fig. 5. (a) Test structure with overlapping metallic layers. The superimposed arrows indicated the direction of linear scanning. (b) shows the process stackup, indicating the metal layers. (c) Plot of the resonant frequency as calculated from the measured phase of S_{12} .

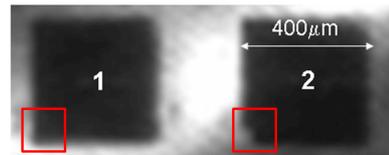


Fig. 6. A broadband incandescent IR source was used to illuminate the chip from the back-side, and a broadband IR camera was used, with a lens, to record the image of two $400 \mu\text{m}$ square circuit regions of a large CMOS chip fabricated in a standard IBM process. The square indicates the scan area.

1.8 GHz, are shown in Fig. 7. Each scan was normalized using its respective spatial-global maximum. The normalization factors for circuits 1 and 2 were 650.48 and 648.05, respectively. After the data was registered using cross-correlation, to account for alignment imperfections, a pixel-based image subtraction was performed on pairs of 2D scans to identify local differences. Prior to registration, the scans are upsampled according to the scan step size to make a single pixel equivalent to $1 \mu\text{m}$. The upsampling enables more accurate registration. The spatial interpolation used was a weighted average of neighboring 4×4 pixels. The separation between the blue and red lines in Fig. 7(b) indicates the system is able to probe buried metallization content.

A different CMOS chip with busses on the top metal layers was used as a third test structure with the same probe circuit, but scanned at $20 \mu\text{m}$ height. Because of this scan height, the effective probe footprint, and thus the resolution, is approximately $20 \mu\text{m}$. The bus feature of approximately $10 \mu\text{m}$ is identifiable and marked by dashed lines in Fig. 8(a). The results suggest that extraction of features below the typically

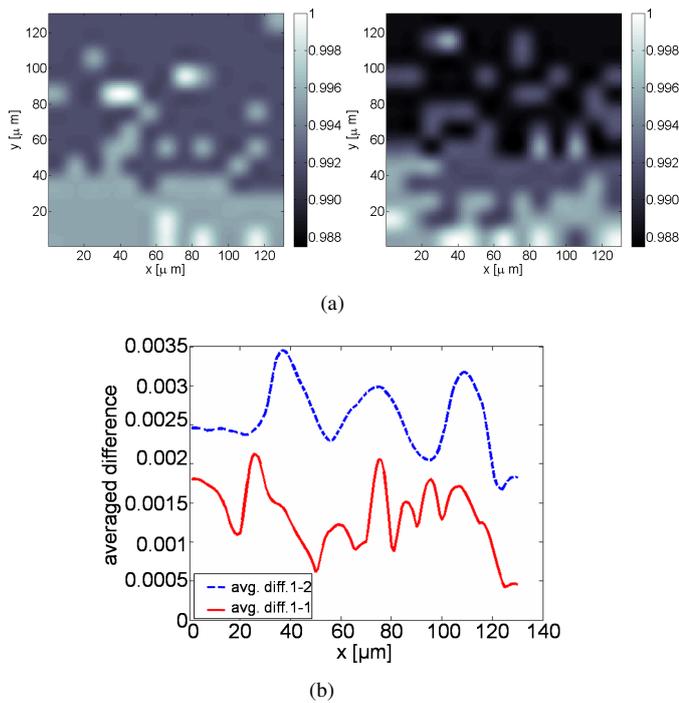


Fig. 7. (a) Measured normalized Q-factor for circuit 1 (left) and 2 (right) from Fig. 6(a). The scan area corresponds to the superimposed rectangles in Fig. 6. (b) Average difference in normalized Q-factor plotted as a function of x , averaged over all pixels in the y -direction. The dashed blue line indicates the difference of normalized data between circuit 1 and 2. The solid red line shows the difference of normalized data in two scans of circuit 1.

accepted theoretical resolution of $20\ \mu\text{m}$ is possible. We are limited to the scan step size ($7.5\ \mu\text{m}$) as a possible resolution of the probe circuit but finer structure on the order of a few microns is visible on the bus structure so it remains to be seen how much lower than the theoretical resolution we can achieve. Note that the free-space wavelength (λ_0) for this probe circuit is $16.7\ \text{cm}$ so we have shown resolution in the range of $\lambda_0/10,000$. An optical image of the scan area is shown in Fig. 8(b) for comparison.

V. CONCLUSION

This paper demonstrates a compact microstrip high-Q microwave probe circuit for near-field profile characterization with feature detection of a few microns (limited by the scan step size) at $1.8\ \text{GHz}$ using a $15\text{-}\mu\text{m}$ probe tip placed $5\text{-}20\ \mu\text{m}$ above a quasi-planar sample. GaAs and CMOS test samples with multiple dielectric and metal layers are characterized. The probe circuit and probing setup can be extended to arrays of probes, multi-frequency and multi-resolution probing, and active circuit integration within the probe circuit, is possible in the future.

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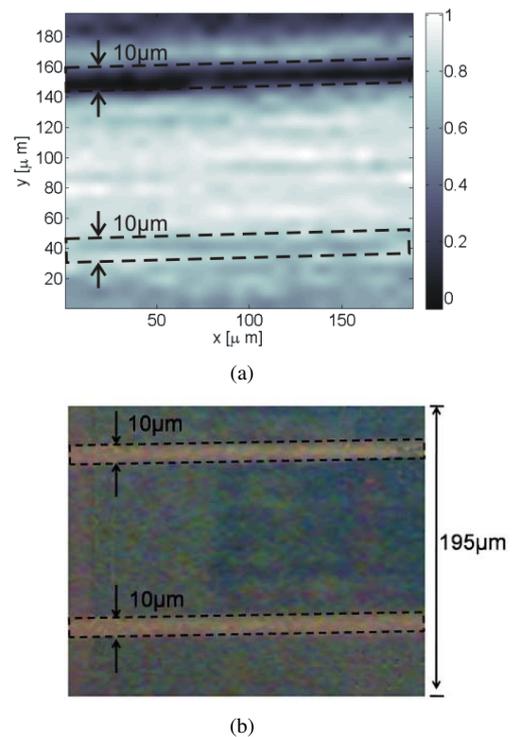


Fig. 8. (a) Measured normalized resonant frequency for a 2D scan over the bus wires of a CMOS integrated circuit, with the corresponding micrograph (b). The bus wires are $10\ \mu\text{m}$ across, suggesting sub-resolution feature detection.

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