Microwave Packaging for Voltage Standard Applications

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***Abstract*—Improved packages for Josephson Voltage Standard (JVS) circuits have increased operating margins, reliability, and longevity of JVS systems. By using the "flip-chip-on-flex" technique, reliable chip and cryoprobe mounting have been demonstrated. The microwave structures on these packages have been improved such that more power can be delivered to the JVS chip over a wider frequency range: DC to over 30 GHz. Detailed finite-element simulations were performed to optimize the chip-to-flex launches as well as the on-flex transmission lines. It was found that coplanar waveguide transmission line designs had improved insertion and return losses compared to those of the microstrip transmission line designs, in large part due to the large discontinuities associated with through-substrate vias for microstrip ground connections. The improved coplanar-waveguide package/probe yielded insertion loss dominated by the ∼0.25 dB/GHz cable loss and VSWR better than 2:1 for the entire 0–30 GHz band. Substantially larger JVS system operating margins were measured using the coplanar-waveguide package; for a 5120 junction array a quantized voltage step greater than 1 mA bias current range is shown for a 10–30 GHz band.**

***Index Terms*—Cryogenic electronics, integrated circuit packaging, Josephson arrays, Josephson device packaging, superconducting device packaging, superconducting integrated circuits, superconducting microwave devices.**

I. Introduction

THIS WORK addresses the refinement of microwave packaging technology for a superconductive Josephson voltage standard (JVS) chip directly soldered to a flexible carrier. The primary design considerations for these cryo-packages are long service life, improved microwave performance, and stable, reliable chip-to-carrier contacts. For the past 10 years [1], the National Institute of Standards and Technology (NIST) has been designing and fabricating a variety of circuits based upon superconductor-normal metal-superconductor (SNS) Josephson junction (JJ) technology including chips for programmable Josephson voltage standards (PJVS) [2]–[5] and pulse-driven AC Josephson voltage standards (ACJVS) [6], [7]. Recent efforts have been focused on increasing the bias-current operating margins and long-term reliability of these devices so that they may be used for many years in their respective applications.

To resolve chip-contact reliability issues in previous-generation CuBe spring-finger based JVS systems, a "flip-chip-on-flex" method of permanently bonding JVS chips to a flexible cryo-package was developed and discussed thoroughly in [8]. This technology utilizes InSn solder to directly attach the bond pads on the 1 cm × 1 cm JVS chip to traces on a flexible microwave substrate, hereafter referred to as "flex". This robust and repeatable structure is capable of absorbing the thermal expansion of the silicon chip when it is cycled many times between room temperature and 4 K. Building upon the previous work in [8], this work presents a redesign of the microwave aspects of the package. By use of improved components and coplanar waveguide (CPW) geometry optimized using full-wave simulations, the usable bandwidth of the microwave package has successfully been extended from DC to 30 GHz. An example of a JVS chip bonded to microwave-optimized flex is shown in Fig. 1.

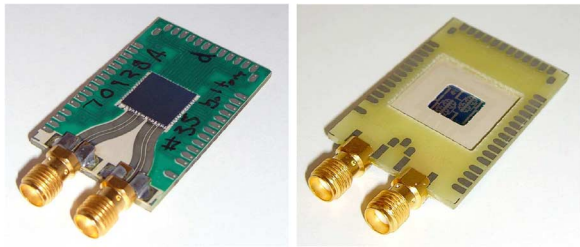

Fig. 1. Photographs, top and bottom, of the optimized flip-chip-on-flex microwave package with a microwave test structure chip mounted. Left: flex side, showing CPW microwave launches and DC bias/output lines. Right: chip side, showing chip (center), flip-chip bonded to flex (surround), and FR4 mechanical stiffener (outer).

The improved microwave bandwidth of this package has been an enabling technology for a 20% improvement in the output voltage of the broadband-pulse-waveform-driven ACJVS system to 275 mV rms [6], [7]. For the PJVS systems, the extension of the operational bandwidth of the package has allowed the 10 V PJVS in development to be targeted at 20 GHz rather than 16 GHz, thus reducing the junction count by 20% [5].

II. Microwave Package Optimization

The microwave package can be broken down into several functional blocks relating to design choices. First, there is the connector itself; low cost, broad bandwidth to greater than

Manuscript received August 26, 2008. First published June 26, 2009; current version published July 10, 2009. This work was supported in part by CU-NIST research symposium seed funding for collaborations, and a Department of Education GAANN fellowship in Hybrid Signal Electronics at the University of Colorado.

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Digital Object Identifier 10.1109/TASC.2009.2018766

20 GHz, and mechanical robustness are critical features. Next, the choice of microwave substrate determines transmission-line geometry, affects loss, and must allow enough flexibility to absorb the differential thermal expansion of the Si chip. The flex-to-chip interface must maintain mechanical stability and electrical repeatability without sacrificing microwave performance. Finally, the on-chip pad geometry must be large enough to bond repeatedly, small enough to keep the I/O count high, and backwards-compatible with legacy designs at a reduced level of performance for testing purposes. All of these factors of the package must be optimized to achieve a broadband, well matched, microwave feed to the chip.

The previous flip-chip-on-flex package used a low-cost, off-the-shelf, edge-mount SMA connector and a 50 μm-thick Cu microstrip (MS) transmission line on 250 μm-thick, Rogers RO3003 [9] substrate. The standard edge-mount connector, while providing good mechanical stability, degraded in microwave performance quickly above 16 GHz. The choice of MS transmission lines required the use of through-substrate vias to make the ground connections at the chip and connector. The inductance of these vias introduced several strong resonant bands at which the feed exhibited large reflections, and consequently very little microwave power was delivered to the JVS chip.

In the optimized design, CPW transmission lines were selected to eliminate the need for through-substrate vias. The Johnson 142-0761-891 [9] precision SMA connector, optimized for fine-dimension CPW to 26.5 GHz, was identified as a good compromise between the additional expense and mounting complexity of a 3.5 mm connector, and the unacceptable performance of a standard edge-mount SMA connector. To better match the flex CPW to the chip pads and the connector geometry, a higher-dielectric substrate was desired. Rogers RO3006 [9] in 250 mum thickness was chosen, trading slightly less stability of the dielectric constant over temperature for better manufacturability of 50 Ω CPW dimensions.

Initial layout geometries were obtained using canonical, closed-form CPW models, then simulated and refined as single transmission line elements of uniform-cross-section using Ansoft's HFSS [9] 3-D finite-element-method (FEM) simulator. The single-segment HFSS results were integrated in a complete HFSS simulation for final adjustments. Fig. 2 shows the three-dimensional geometry of the flip-chip-on-flex package. Solder bump reflow was modeled to first order as a trapezoidal connection from flex-pad edge to chip-pad edge. The HFSS simulation results from the model shown in Fig. 2 were cascaded in a circuit simulator with ideal lossy transmission lines calculated from the HFSS port impedances to represent the 1.2 m PFTE coaxial cable and the 6.4 mm on-chip transmission lines. Fig. 3 shows the results of the circuit simulation compared with measured results discussed in Section III.

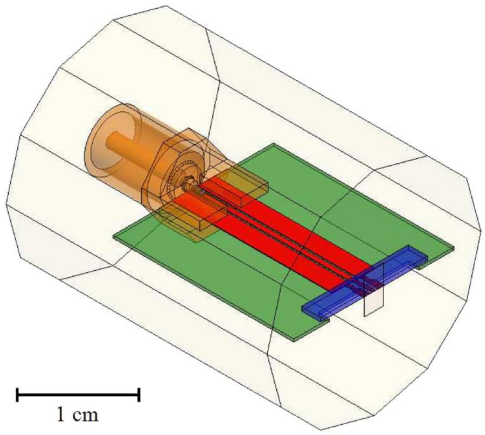

Fig. 2. Broadband flip-chip-on-flex interface model in HFSS. From left to right, yellow is the FEM domain boundary, orange is the Cu connector, white is PTFE, green is the RO3006, red is copper traces, yellow is InSn solder, blue is the Si chip, and maroon is Nb traces on-chip.

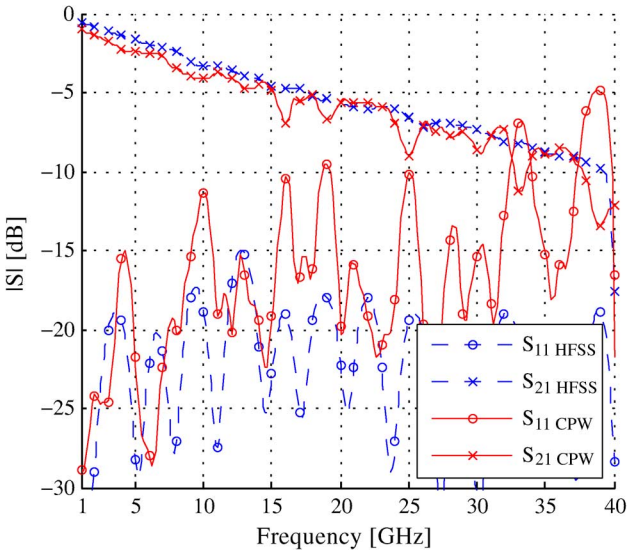

Fig. 3. Simulated scattering (S) parameter performance of optimized CPW flex to chip launch, in blue dashed lines, compared to measured cryoprobe with CPW flex through line results from Section III, in red solid lines.

III. Testing

In order to test the optimized package structure, 1 cm $\times$ 1 cm chips were fabricated on a Si wafer with a through-connected, 50 Ω, 6.4 mm long, superconducting Nb CPW transmission line between two optimized microwave launches. These were flip-chip-bonded to the optimized flex carrier using the process described in [8]. For comparison, identical through-line chips were packaged using the legacy MS flex design. These packaged chips were installed in a 1.2 m cryoprobe utilizing 3.58 mm semi-rigid coaxial cable with solid PTFE dielectric, copper conductors, and SMA connectors to reach the bottom of a liquid He dewar at 4 K.

Measurements were performed with an Agilent 8722ES [9] vector network analyzer (VNA). The calibration reference plane was set at the room-temperature end of the cryoprobe using an Agilent 85052C [9] Short-Open-Load-Through (SOLT) calibration kit. Figs. 4 and 5 show a comparison by package of the measured cryoprobe insertion loss, IL, (power lost through the device) and return loss, RL, (power reflected off of the device), respectively. The optimized CPW flex has all but eliminated the power dropouts that plagued the MS flex design at 13, 17, 19, and 21 GHz, and above 22 GHz. These lossy bands prevented the ACJVS system from working in the MS package with 5000 or more JJs. The dominant slope of the through IL versus frequency measurement corresponds to the measured

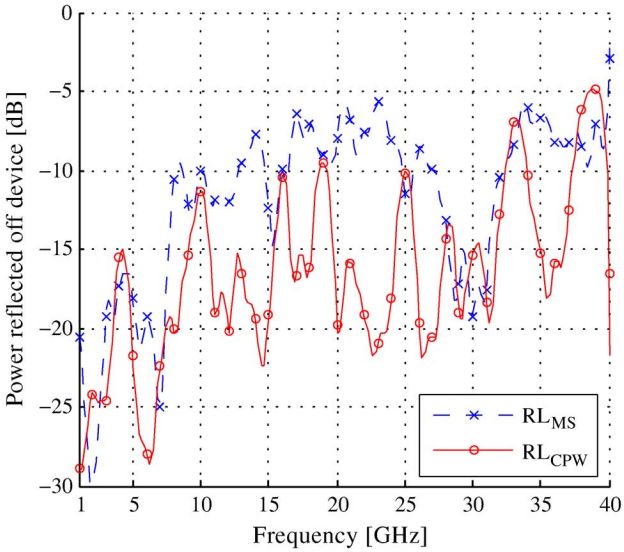

Fig. 4. Measured cryoprobe IL, using room-temperature SOLT calibration, of MS legacy flex package in blue dashed lines, and CPW optimized flex package in red solid lines.

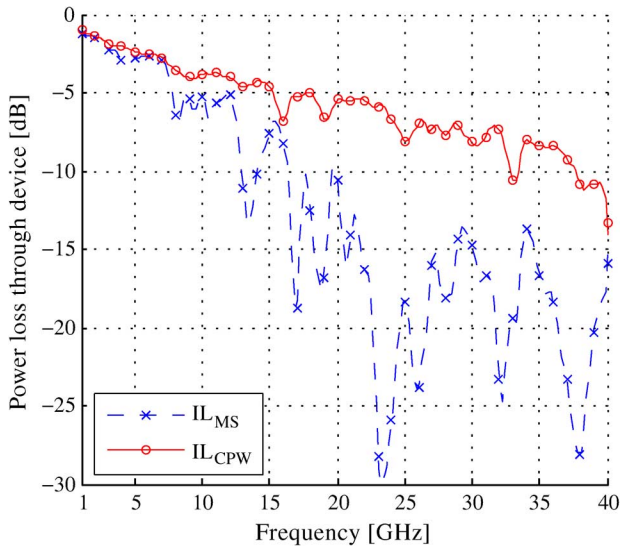

Fig. 5. Measured cryoprobe RL, using room-temperature SOLT calibration, of MS legacy flex package in blue dashed lines, and CPW-optimized flex package in red solid lines.

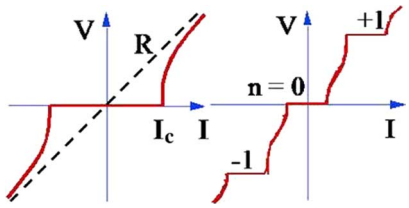

Fig. 6. JJ I-V curves, with DC bias only (left) and with microwave excitation (right). The voltage summation of many single JJ I-V curves yields the array IV performance. The array $n = 0$ step suppression below I_C indicates maximum single JJ microwave power, and $n = |1|$ step current breadth indicates microwave power uniformity across all the JJs in the array.

TABLE I
PIECEWISE LINEAR POWER FUNCTIONS. SOURCE OUTPUT POWER IS THE COMMAND WAVEFORM IN THE LEVELED SYNTHESIZER RANGE. APPROXIMATE ON-CHIP POWER IS CALCULATED BY APPLYING MEASURED SYSTEM GAIN TO THE SWEEPER OUTPUT POWER FUNCTION

Frequency	10 GHz	15 GHz	20 GHz	25 GHz	30 GHz
Source Output Power	–13.0 dBm	–10.0 dBm	–10.0 dBm	–10.0 dBm	–8.0 dBm
Approximate On-chip Power	10.0 dBm	12.5 dBm	11.0 dBm	10.5 dBm	9.0 dBm

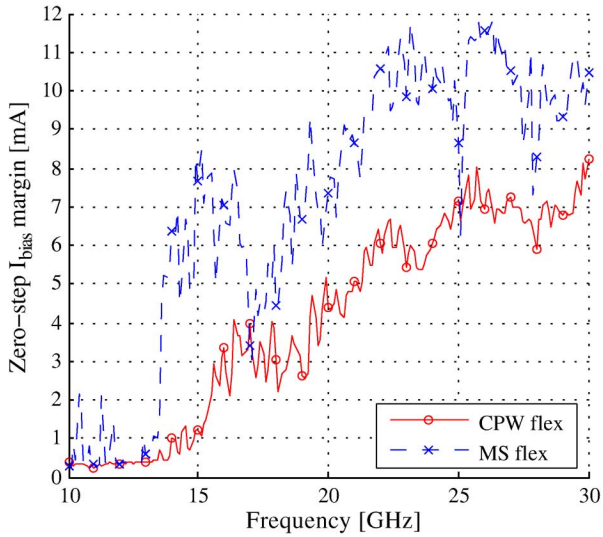

Fig. 7. Measured zero-step current bias magnitude of 5120-JJ arrays on two identical ACJVS chips mounted in different "flip-chip on flex" packages. The improved CPW package data set is shown in red solid lines marked with ∘; the legacy MS package data set is shown in blue dashed lines marked with ×. Zero-step suppression below I_C of 11.5 mA is an indication of absolute microwave power reaching any one junction in the array.

frequency-dependent loss of the PTFE cables. Neglecting this slope, the CPW flex has no dropouts larger than −3 dB from DC to 30 GHz. The entire CPW cryoprobe system is matched to better than 2:1 VSWR over the entire 0–30 GHz bandwidth.

A figure of merit for the power and uniformity of the microwave excitation of the Josephson junction array is the range of DC bias current for which the JJ Shapiro DC voltage steps are quantized. This DC bias range, or current margin, is measured with a DC I-V sweep under microwave excitation, as shown in Fig. 6. The suppression of the zero-voltage step below I_C (11.5 mA for these chips) is an indication of the microwave current through any one junction. A quantized $n = |1|$ step over a larger bias current range is an indication better microwave current uniformity through the entire array. A larger bias current range on a step makes the JVS system more immune to noise and allows it to source or sink more current in a measurement while remaining quantized, defining the operating margins of the system. For ACJVS systems the JJ array needs to respond in a uniform manner over the broad bandwidth of the 10 Gb/s pulsed Delta-Sigma drive waveform [7].

In order to evaluate real array performance, two pre-screened, identical 5120-JJ array ACJVS chips were mounted using the CPW and MS flex mounts, then evaluated for current margin versus frequency. The microwave excitation power was ramped over frequency to maximize the one-step on the CPW flex chip mount, compensating for amplifier gain, cable loss, and junction response. The piecewise-linear power ramp frequency corner points are shown in Table I. The MS flex chip data sets are taken using the same power ramp for a direct comparison with the improved CPW flex. Figs. 7 and 8 show the resultant zero-step and

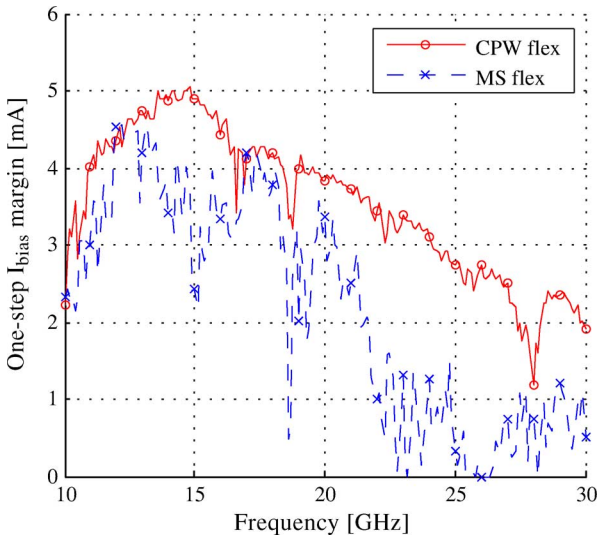

Fig. 8. Measured one-step current bias magnitude of 5120-JJ arrays on two identical ACJVS chips mounted in different "flip-chip on flex" packages. The improved CPW package data set is shown in red solid lines marked with ∘; the legacy MS package data set is shown in blue dashed lines marked with ×. A larger one-step magnitude is an indication of better microwave power uniformity across all the junctions in the array.

one-step current margins, respectively. Consistently improved bias current margins over the entire band are shown with the CPW flex mounted chip. The 19 GHz and 28 GHz resonant dropouts in the one-step and zero-step using both packages are the second and third resonance of the array length on chip. The 90 MHz standing wave apparent in this finer sweep is due to resonant length of the 1.2 m cryoprobe coax. When tested in the ACJVS system under pulsed excitation, the MS packaged chip exhibited 1.4 mA of bias margin while the CPW packaged chip had more than double the current margin at 3.0 mA of quantized range for a 5120-JJ array.

IV. Conclusions

The CPW flex is a considerable enhancement to the legacy MS flex design, especially above 16 GHz, where insertion and return losses are improved by nearly an order of magnitude, providing substantially more microwave power on-chip. Access to 0–30 GHz bandwidth of the CPW flex has enabled permanent flex-mounting of ACJVS chips. The limited bandwidth, large reflections, and lossy dropouts of the legacy MS package did not provide adequate pulse-waveform power levels on chip to operate the 5120-JJ array ACJVS system.

Very broadband, mechanically robust microwave packaging technology for JVS applications has been demonstrated. This packaging technology using precision SMA microwave connectors, CPW transmission lines on a low-loss microwave substrate, and flip-chip-on-flex bonding technology exhibits improved microwave performance from DC to above 30 GHz. The reliability and performance gains of these packages over legacy designs are an enabling technology for NIST ACJVS and 10 V PJVS systems. Future improvements may be realized by tackling the reliability, standing-wave, and loss challenges in the cryoprobe.

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[9] This commercial tool is identified in this paper only in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment identified are necessarily the best available for the purpose.