Adaptive Tuning for Handheld Transmitters

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***Abstract*—This paper presents a closed loop impedance tuner for a WCDMA handset power amplifier, with the goal of increasing overall efficiency by reducing the reflected power when the antenna is mismatched. A self-assessment circuit provides the feedback signal. A directional coupler between the amplifier and the antenna routes the reflected power to a detector where it is compared to the incident power. The output signal from the detector is digitized and fed to a FPGA containing the control algorithm for impedance tuning. The tuner is a simple varactor double-stub design and provides VSWR < 3 at 1.95 GHz for loads with a mismatch up to VSWR = 81. The tuner exhibits loss as low as 0.3 dB and uses two separate control voltages between 0 and 6 V.**

***Index Terms*—impedance matching, varactor tuners, power amplifiers, antenna mismatch, double-stub tuner**

I. Introduction

Impedance tuners have been implemented with solid-state and MEMS devices for a variety of applications ranging from low gigahertz to millimeter wave frequencies. The majority of low-loss MEMS-based tuners were demonstrated between 20-40 GHz [1], [2], [3], [4], [5] for impedance matching at fixed frequencies. In [6] a MEMS switched tuner in an intelligent power amplifier (PA) demonstrated frequency tuning of peak power between 8 and 12 GHz. Solid-state tuners have also been demonstrated, e.g., a MMIC narrow-band tuned amplifier at 27 GHz with FET switches [7]. At lower frequencies (2 GHz), a varactor-based tuner with Si on glass technology was designed for improving amplifier distortion [8].

The motivation of this work is to reduce the mismatch between an RF power amplifier (PA) and an antenna in a mobile application using a simple tuner with inexpensive technology. Typically there is a circulator/isolator at the output of the PA protecting it from power reflected from the antenna. The downside of this approach is that any reflected power is dissipated, which is a waste of power. With a matching network, more power can be delivered to the load and the PA requirements relaxed. Therefore, replacing the hybrid isolator with an electronically tunable component has the potential for improved system efficiency and better system integration. In high VSWR conditions, the supply voltage to the PA must be increased to maintain required operating conditions. Instead of setting the supply voltage to a conservatively high value, the knowledge of instantaneous VSWR can empower a control circuit to reduce the supply voltage during low-VSWR situations and therefore reduce the losses of the PA, which is not possible with just an isolator.

A block diagram of a mobile application transmit path is shown in Fig. 1. The output of the PA is fed into a bi-

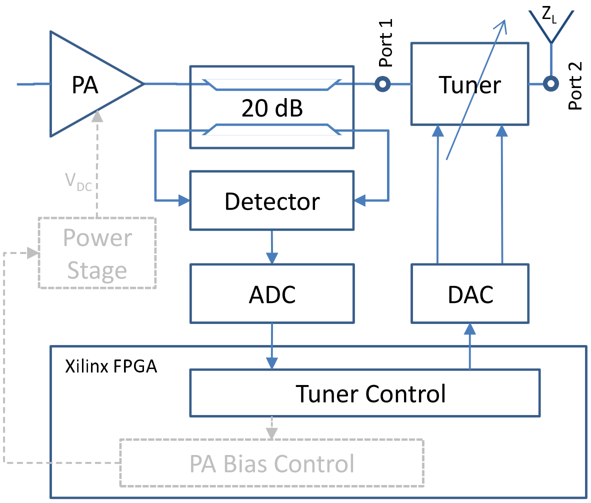

Figure 1. Block diagram of a WCDMA closed-loop tuned PA. The reflected power from a mismatched antenna is detected and digitized. The adaptive algorithm is implemented in the Xilinx FPGA and a control signal sent to both the tuner and the supply control stage.

directional coupler, from which the incident and reflected powers can be detected. Any mismatch at the antenna produces a signal at the output of the detector which is digitized by the ADC and then processed by the FPGA, providing control signals back to the tuner, and to the adaptive DC supply circuit. With this architecture, the reflected power from the antenna is not lost as in the case of a circulator/isolator, thus improving overall system efficiency. Another important role of the tuner is to protect the PA and, in conjunction with the control of the PA bias, preserve linearity. Although the impedance tuner alone helps improve efficiency, the true benefit is gained with a system which integrates the DC power stage.

This paper focuses on the design, implementation, and characterization of a varactor-based impedance tuning network, and also presents the circuit components required for closed-loop efficiency and linearity improvements for handheld WCMDA PAs.

II. Tuner Design and Characterization

The tuner design chosen for this work is a double-stub architecture with two low cost varactor diodes as shown in Fig. 2. The first step in the design process is to select a suitable varactor diode. A sampling of packaged varactors was measured in a microstrip one port circuit using an HP 8510C VNA with a TRL calibration and multiple reverse bias

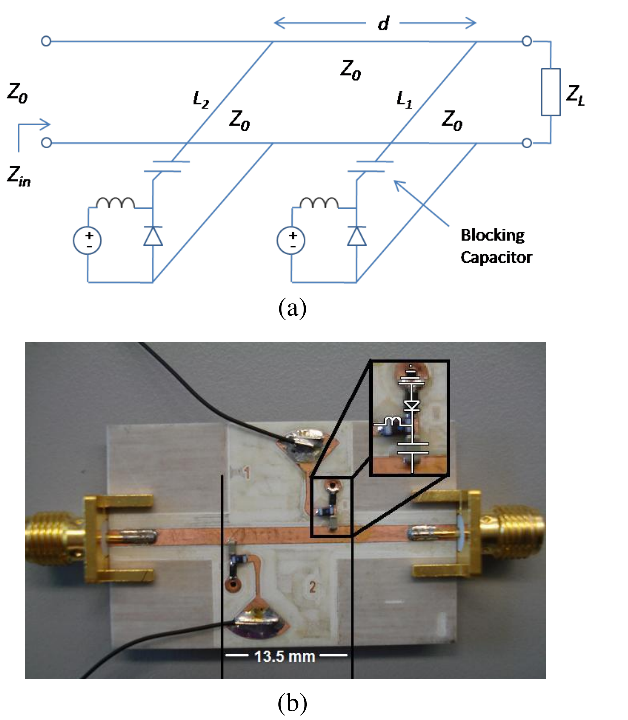

Figure 2. (a) Circuit diagram of double-stub tuner with a varactor diode at the end of the two shunt stubs and (b) a photo of the tuner circuit (13.5 mm x 23.5 mm) fabricated on 32 mil RO4003 substrate.

voltages. The inductance of the anode ground via is included in the measured diode model because it is the configuration in which the diode will be used. The Skyworks 1405 abrupt junction tuning varactor was chosen because of its high Q, large tuning ratio, and low capacitance.

The tuner design involved a compromise between tuning range and sensitivity due to component tolerances. With a double-stub tuner, where all the lines are of characteristic impedance Z_0, there is a range of impedances that cannot be matched. They correspond to a circular region tangent the edge of the Smith chart, whose radius depends on the distance d between the stubs. The shorter the distance, the larger the tuning range. Typically, d is set to $\lambda_g/8$ but for this design it was shortened to $\lambda_g/10$ to increase the tuning range.

In mobile handsets, antennas are matched to $50\,\Omega$ under nominal conditions, but they vary with near-field loading. Based on cell phone antenna measurements [9] we expect the antenna VSWR to be as high as 4:1 at 1.95 GHz (see Fig. 3). This tuner should match loads centered around $50\,\Omega$ with VSWR of 1.5:1 or better. With d chosen, from standard transmission line equations one can calculate nominal stub capacitances, which are equal for $Z_L = Z_0$ and given by the following simplified equation:

$$C = \frac{1}{\pi f \cdot \tan(\beta d)} \qquad (1)$$

When f = 1.95 GHz and $d = \lambda_g/10$, the required shunt capacitance for both stubs is roughly 4.5 pF. There are multiple solutions for the stub lengths, and we chose the shortest one for larger bandwidth and smaller physical size. The relationship between open-circuited stub length L and capacitance (without

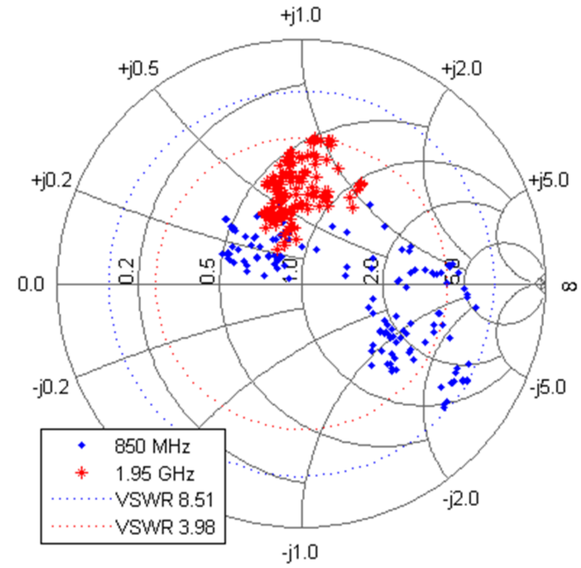

Figure 3. Measured impedance variations of a Nokia 6010 cell phone antenna under various near-field loading conditions (near head, covered by hand, on metal table, etc.).

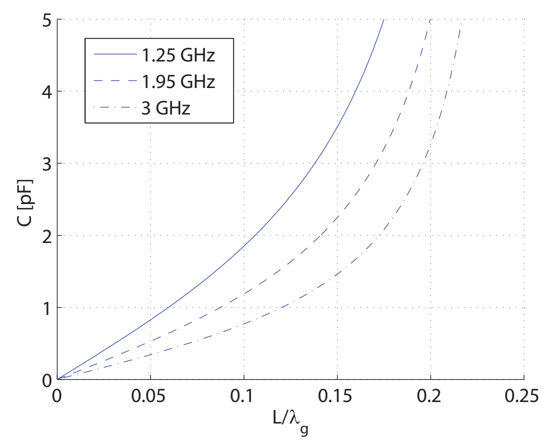

Figure 4. Equivalent capacitance of a $50\,\Omega$ open microstrip stub vs. its electrical length. For stubs shorter than a quarter wavelength, the stubs are capacitive.

any substrate-dependent open-circuit correction) is given by:

$$\frac{L}{\lambda} = \frac{1}{2\pi} \arctan(2\pi f \cdot C \cdot Z_0) \qquad (2)$$

as shown in Fig. 4 . Given this relationship between capacitance and length, one can see that a stub can be completely replaced with a capacitor to save space if one is willing to accept a small amount of additional loss (due to the parasitics of the capacitor). With a varactor-loaded stub, increasing the reverse bias voltage leads to a decrease in the capacitance which effectively shortens the stub length and changes the effective impedance of the tuner transmission line segment.

Starting with the measurement-based varactor model, the double-stub tuner circuit was simulated in AWR Microwave Office, showing the tuning range in Fig. 5. Each tuner stub was swept across 25 bias points, from 0 to 6 V, which results in the 625 points of simulated load-side reflection coefficient S_{22}.

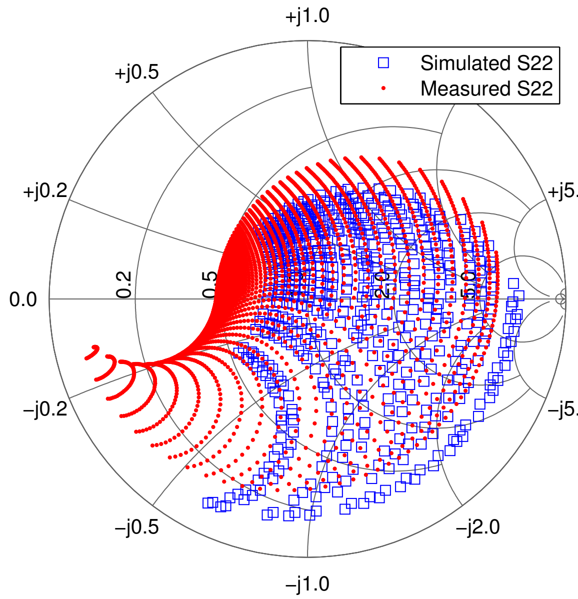

Figure 5. Simulated and measured tuner output impedance at 1.95 GHz as the reverse bias voltages are individually varied from 0 to 6.

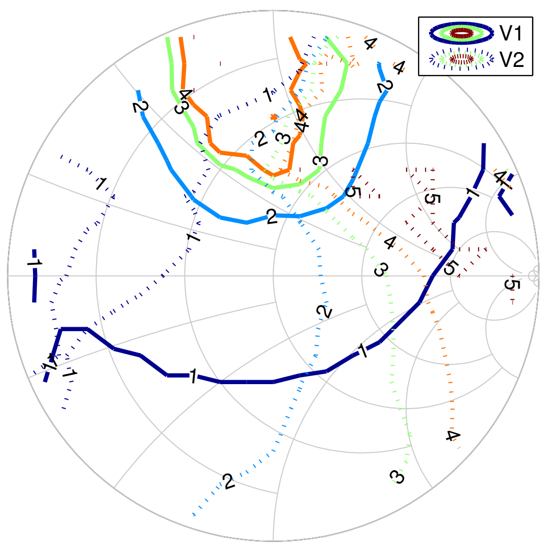

Figure 6. Measured varactor bias voltages V1 and V2 for the best match to a given load impedance at 1.95 GHz

The S_{22} of a tuner shows the complex conjugate of the loads that can be perfectly matched to maximize power transfer. However, the practical tuning range is larger than the Smith chart area covered by S_{22} because the points represent only those loads which can be perfectly matched. If a VSWR of 3:1 is acceptable for the system, the tuning range increases. The measured S-parameters with bias voltages swept in 0.1 V increments, Fig. 5, show good agreement with simulations.

The varactor bias voltages were determined by connecting the tuner to known loads and searching for the tuner state that resulted in the least reflected power. The resulting lookup table of voltages, represented in Fig. 6, is loaded into the FPGA.

An important aspect of an impedance tuner is the insertion loss. In order to calculate tuner loss, we must make some

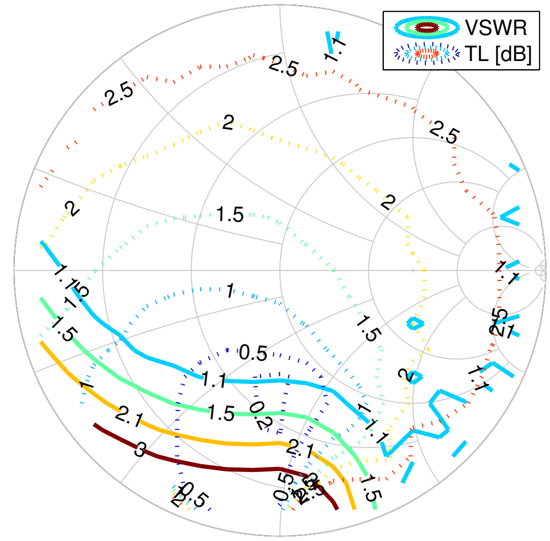

Figure 7. Measured tuner VSWR and TL at 1.95 GHz. While nearly the entire Smith chart can be reduced to VSWR of 3 or better, the insertion loss can be as high as 3 dB. Therefore, this tuner is best suited to match low-impedances that are capacitive.

assumptions. The standard definition for insertion loss in dB is an indication of dissipated/radiated power inside a two port network, given by:

$$IL = 10 \cdot \log\left(\frac{|S_{21}|^2}{1 - |S_{11}|^2}\right) \tag{3}$$

While dissipated power should be minimized in any tuner, power lost due to reflections at port 1 is also important to account for. Since the goal of any tuner is to be matched to its load at port 2, we define a more relevant tuner loss, TL as:

$$TL = 10 \cdot \log\left(\frac{|S_{21}|^2}{1 - |S_{22}|^2}\right) \tag{4}$$

Fig. 7 shows TL and VSWR of this tuner, when loads of up to VSWR = 81 are presented at port 2. One can see that TL increases for inductive and lower impedances. VSWR < 1.1 for a wide range of loads, and VSWR < 3 for 96 % of the simulated loads, calculated from the measured S-parameters and simulated load impedances:

$$VSWR = \frac{1 + \left|\frac{S_{12}S_{21}S_L}{1-S_{22}S_L}\right|}{1 - \left|\frac{S_{12}S_{21}S_L}{1-S_{22}S_L}\right|} \tag{5}$$

where $S_L = (Z_L - Z_0)/(Z_L + Z_0)$. For a 50 Ω PA connected through an isolator to a load impedance of 10-j20 Ω, 50 % of the output power would be reflected and dissipated in the isolator. However, replacing the isolator with the tuner results in only about 12 % of the transmit power lost (shown in Fig. 7 as VSWR≃2 and TL≃0.6 dB).

III. Closed Loop Characterization

Referring to Fig. 1, the PA used in this experiment is an Avago WS2512 with up to 27 dB of gain and P_{OutMax}= 28 dBm between 1.92 and 1.98 GHz. The surface mount 20 dB

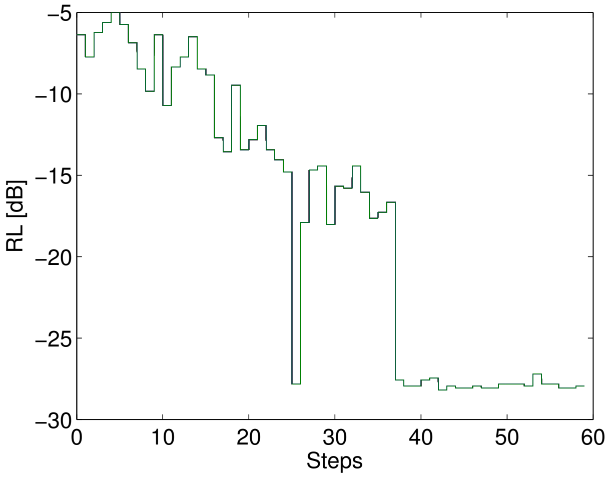

Figure 8. Measured adaptive tuner return loss convergence when the load changes from 50 Ω to 150-j50 Ω

bi-directional coupler has 40 dB isolation. The THS1030 Texas Instruments ADC has 10-bits of resolution at 30 MSPS. The FPGA is a Xilinx Virtex 4 XC4VLX25, which samples the incident and reflected power from the AD8302 gain detector, and the variable load used for testing is a mechanical single slug tuner from Focus Microwaves. The digitized detector output is used by two functional blocks: the tuner algorithm, and the PA bias control.

Initially, the tuner state is set assuming a 50 Ω load. Then the tuner voltages are set for the adjacent impedances (including 48 Ω and 52 Ω as well as other nearby complex impedances) and the FPGA checks to see if VSWR has decreased. If improvement is found, the system then assumes the new load and continues searching adjacent impedances until the state of minimum reflection is found. This searching of adjacent impedances is analogous to the conical scan that antenna tracking systems sometimes use [10]. The algorithm quietly monitors VSWR until a predetermined level of degradation is detected in the match, at which point the system resumes the search. An example of convergence is shown in Fig. 8 in which the load changes from 50 Ω to 150-j50 Ω at step 0.

IV. Discussion

Adaptive tuners and adaptive supplies have been individually used in the past in an attempt to improve system efficiency – the adaptive tuner to decrease mismatch losses, reducing the requirement on the PA, and the adaptive PA supply to reduce DC losses across different PA operating modes. For example, typically V_{DC} = 3.4 V during data transmission, and V_{DC} = 800 mV during voice transmission [11]. In this paper we demonstrate a very simple and cost-effective circuit which improves efficiency due to antenna mismatch. However, integration of the two should provide efficiency improvements greater than the sum of the individual parts.

At high output power, the PA linearity is strongly affected by the antenna environment and the DC supply voltage [12]. The RF envelope at the PA output can saturate a mismatched PA and hence a conservatively high fixed DC supply voltage is generally provided. However, if the tuner control provides VSWR as an input to the PA supply control system, the supply voltage can be reduced to avoid saturating the PA. We believe a simultaneous improvement in linearity and efficiency can be achieved with combined control of adaptive tuning and supply voltage. The practical consideration is whether an increase in overall transmitter complexity is overcome by the overall increased system efficiency. In order to make an assessment of time-averaged efficiency, the probability density function (PDF) for the output power of a WCDMA handheld transmitter needs to be taken into account. In addition, for the impedance tuned PA, the PDF of antenna mismatch should be determined, which will be presented in the future.

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